



N-Channel 20-V (D-S) MOSFETs

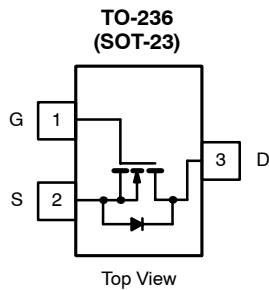
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.4 @ $V_{GS} = 4.5$ V	0.73
	0.5 @ $V_{GS} = 2.5$ V	0.65

FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 4000 V

APPLICATIONS

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems, DC/DC Converters
- Solid-State Relays
- Load/Power Switching-Cell Phones, Pagers



Marking Code: *K2ywl*

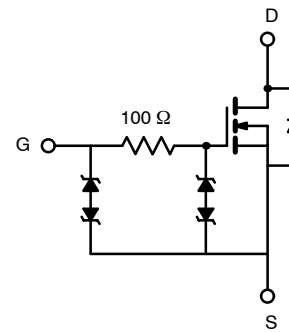
K2 = Part Number Code for TN0200K

y = Year Code

w = Week Code

l = Lot Traceability

Ordering Information: TN0200K-T1—E3 (Lead Free)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^b	$T_A = 25^\circ\text{C}$	I_D	0.73	A
	$T_A = 70^\circ\text{C}$		0.58	
Pulsed Drain Current ^a		I_{DM}	4	
Continuous Source Current (Diode Conduction) ^b		I_S	0.3	
Power Dissipation ^b	$T_A = 25^\circ\text{C}$	P_D	0.35	W
	$T_A = 70^\circ\text{C}$		0.22	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient ^b	R_{thJA}	357	$^\circ\text{C/W}$

Notes

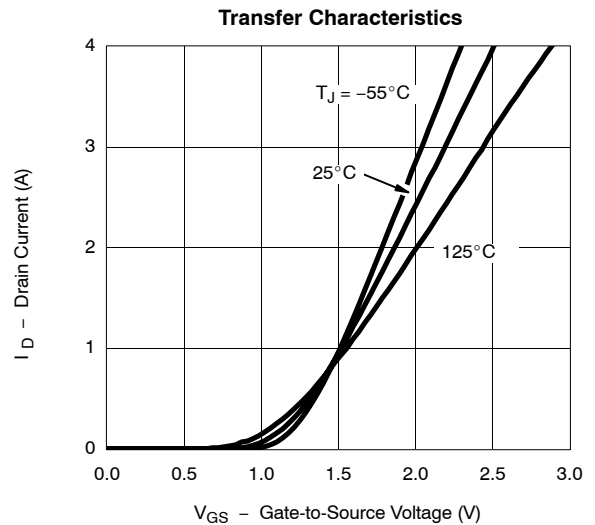
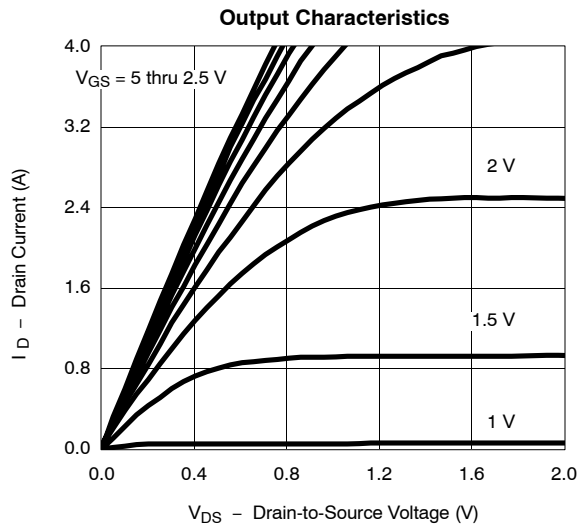
- a. Pulse width limited by maximum junction temperature.
 b. Surface Mounted on FR4 Board, $t \leq 10$ sec.

SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 10 μA	20			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 50 μA	0.45	0.6	1.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V			± 5	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V T _J = 55 °C			1 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	2.5			A
		V _{DS} ≥ 5 V, V _{GS} = 2.5 V	1.5			
Drain-Source On-Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.6 A		0.2	0.4	Ω
		V _{GS} = 2.5 V, I _D = 0.6 A		0.25	0.5	
Forward Transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 0.6 A		2.2		S
Diode Forward Voltage ^a	V _{SD}	I _S = 0.3 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 0.6 A		1400	2000	pC
Gate-Source Charge	Q _{gs}			190		
Gate-Drain Charge	Q _{gd}			300		
Gate Resistance	R _g			105		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 16 Ω I _D = 0.6 A, V _{GEN} = 4.5 V, R _g = 6 Ω		17	25	ns
Rise Time	t _r			20	30	
Turn-Off Delay Time	t _{d(off)}			55	85	
Fall-Time	t _f			30	45	

Notes

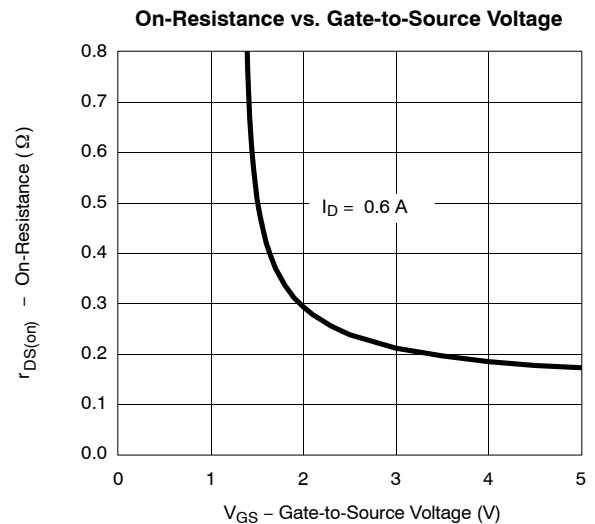
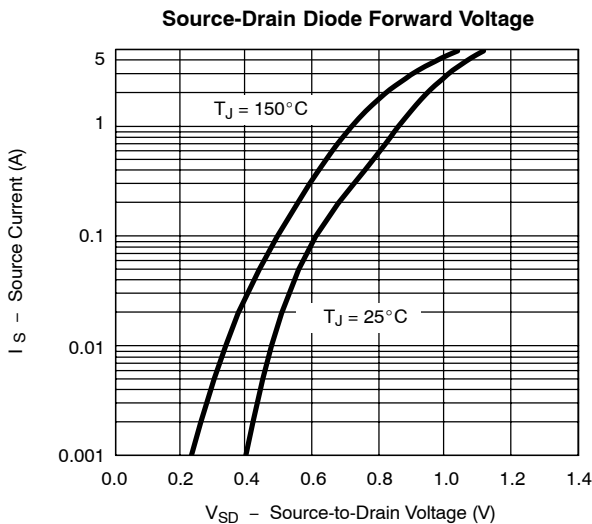
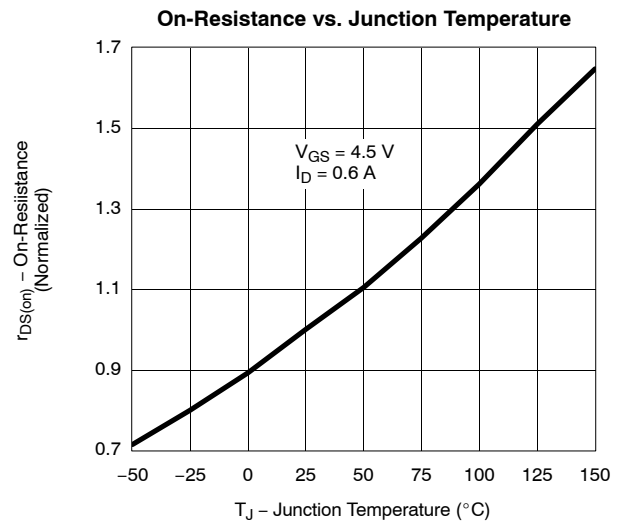
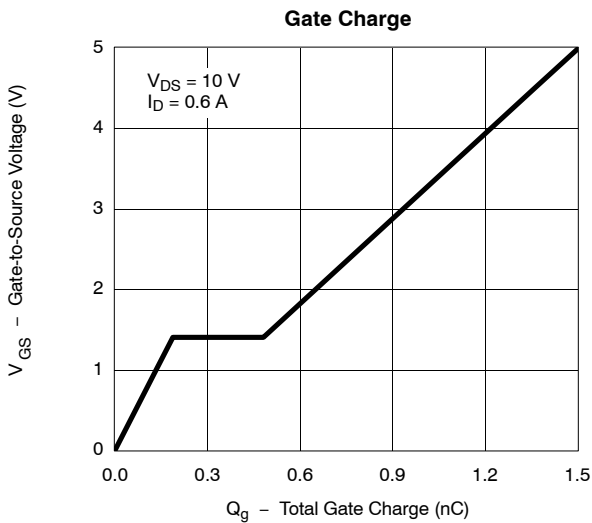
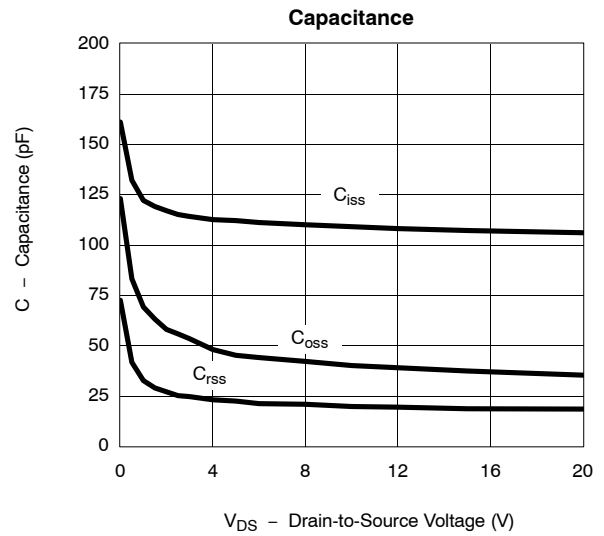
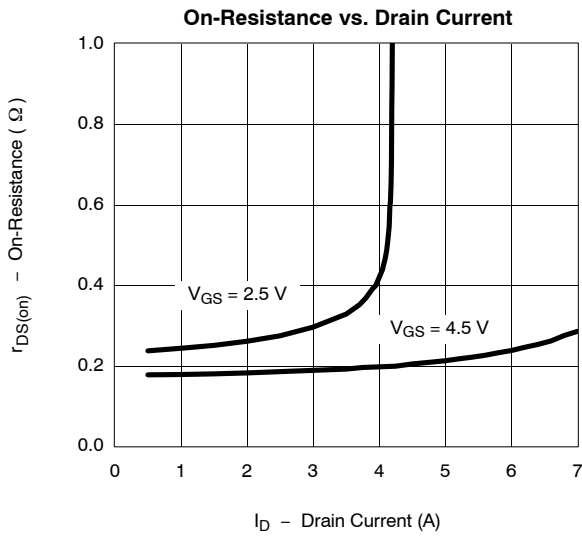
- a. Pulse test: PW ≤ 300 μs duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



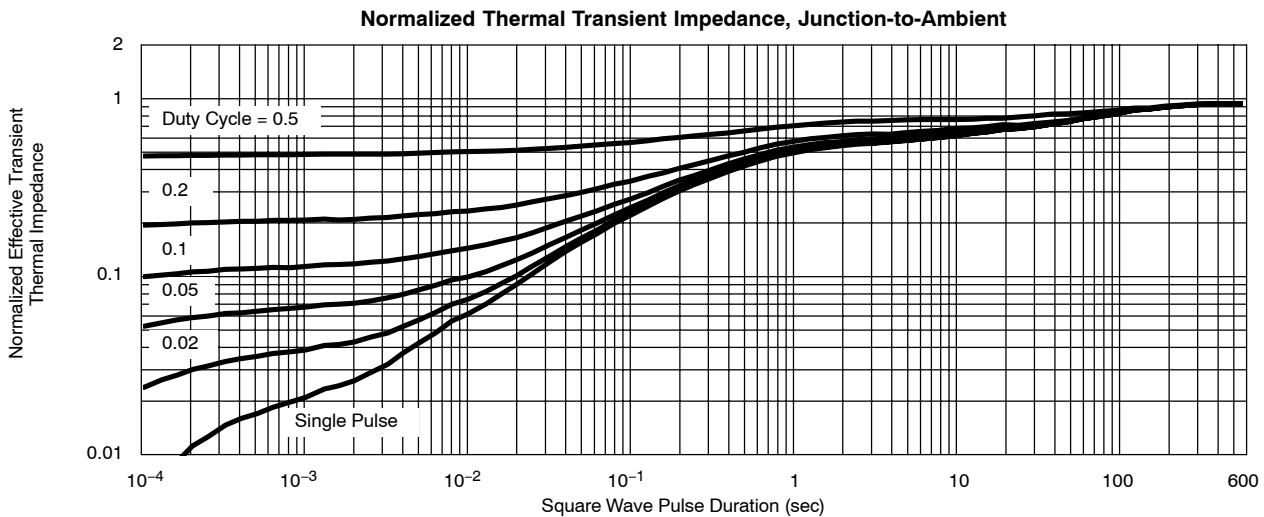
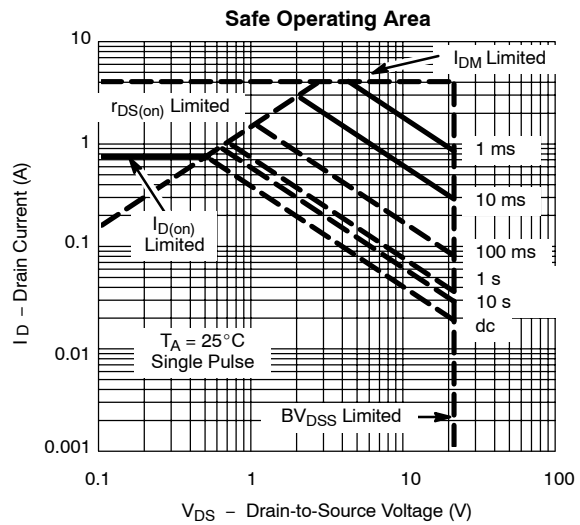
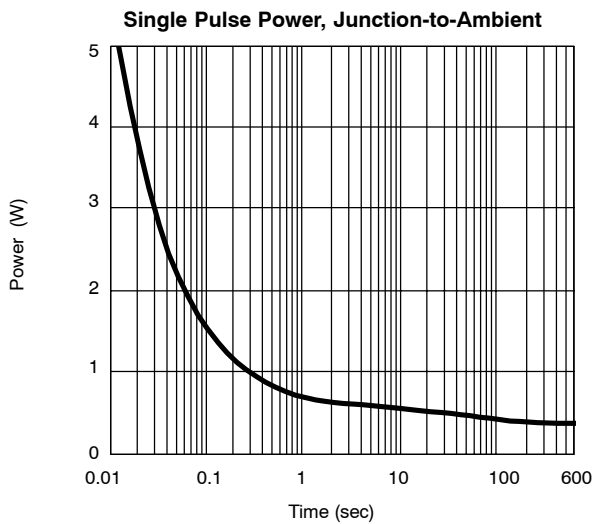
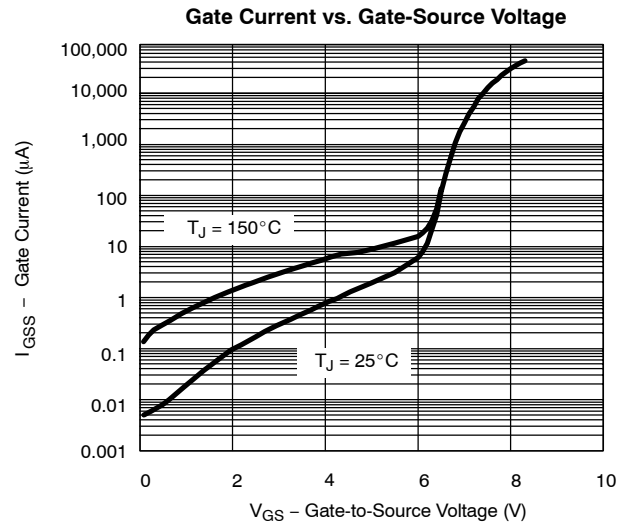
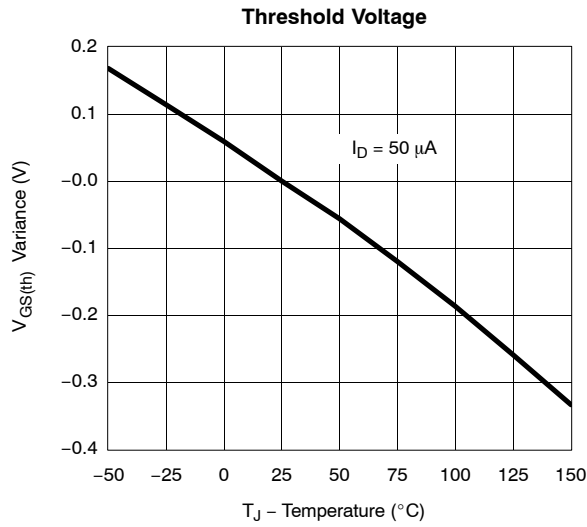


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