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Features

- Embedded EEPROM
  - Very Easy Development with RFPDK
  - All Features Programmable
- Frequency Range: 240 to 480 MHz
- OOK Modulation
- Symbol Rate: 0.5 to 30 kbps
- 1-wire Interface
- Output Power: -10 to +13 dBm
- Supply Voltage: 1.8 to 3.6 V
- Current Consumption: 12.4 mA @ +10 dBm
- Sleep Current < 20 nA
- FCC / ETSI Compliant
- RoHS Compliant
- 6-pin SOT23-6 Package

Applications

- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Remote Fan Controllers
- Infrared Transmitter Replacements
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

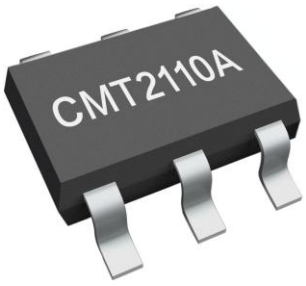
Ordering Information

Part Number	Frequency	Package	MOQ
CMT2110A-ESR	Random	SOT23-6	3,000 pcs
CMT2110A-ESR3	315.00 MHz	SOT23-6	3,000 pcs
CMT2110A-ESR4	433.92 MHz	SOT23-6	3,000 pcs
More Ordering Info: See Page 18			

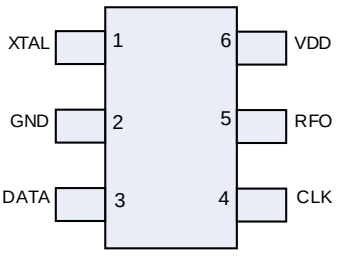
Descriptions

The CMT2110A is an ultra low-cost, highly flexible, high performance, single-chip OOK transmitter for various 240 to 480 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The device only requires 1-wire interface for the external MCU or encoder to send in the data and control the transmission. An embedded EEPROM allows the frequency, output power and other features to be programmed into the chip using the CMOSTEK USB Programmer and RFPDK. Alternatively, in stock products of 315/433.92 MHz

EEPROM programming. The CMT2110A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. The CMT2210A receiver together with the CMT211x transmitter enables an ultra low cost RF link.



SOT23-6



CMT2110A

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Typical Application

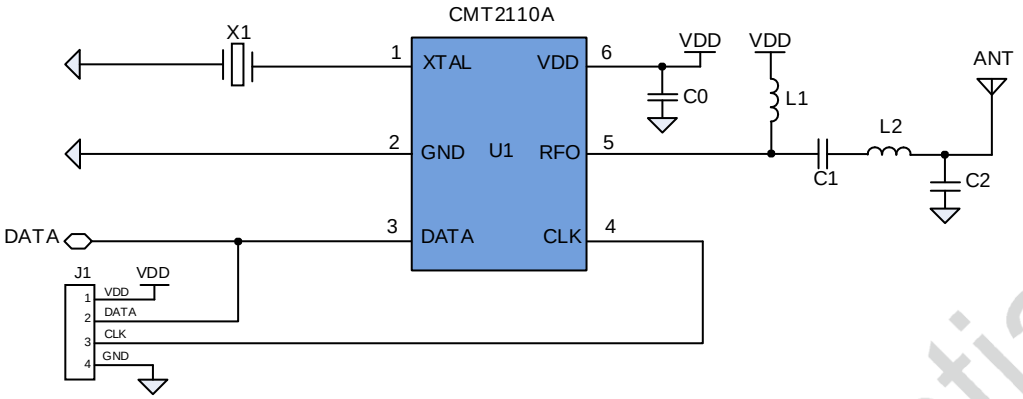

Figure 1. CMT2110A Typical Application Schematic

Table 1. BOM of 433.92 MHz Low-Cost Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2110A, low-cost 240 – 480 MHz OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	27	nH	Murata LQG18

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Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying **BOM**
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

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Table of Contents

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1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 433.92 MHz, output power is +10 dBm terminated in a matched 50 Ω impedance, unless otherwise noted

1.1 Recommended Operating Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		1.8		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

1.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

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1.3 Transmitter Specifications

Table 4. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		480	MHz
Synthesizer Frequency Resolution	F_{RES}			198		Hz
Maximum Output Power	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[2]	t_{RAMP}		0		1024	us
Current Consumption @ 315 MHz	I_{DD315}	0 dBm, 50% duty cycle, 9.6 kbps		6.8		mA
		+10 dBm, 50% duty cycle, 9.6 kbps		12.4		mA
		+13 dBm, 50% duty cycle, 9.6 kbps		16.0		mA
Current Consumption @ 433.92 MHz	$I_{DD433.92}$	0 dBm, 50% duty cycle, 9.6 kbps		6.9		mA
		+10 dBm, 50% duty cycle, 9.6 kbps		13.4		mA
		+13 dBm, 50% duty cycle, 9.6 kbps		17.4		mA
Sleep Current	I_{SLEEP}			20		nA
Symbol Rate	SR		0.5		30	kbps
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise	PN	100 kHz offset from F_{RF}		-80		dBc/Hz
		200 kHz offset from F_{RF}		-82		dBc/Hz
		400 kHz offset from F_{RF}		-92		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Harmonics Output for 315 MHz[3]	$H2_{315}$	2nd harm @ 630 MHz, +13 dBm P_{OUT}		-60		dBm
	$H3_{315}$	3rd harm @ 945 MHz, +13 dBm P_{OUT}		-65		dBm
Harmonics Output for 433.92 MHz[3]	$H2_{433.92}$	2nd harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3rd harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB
Occupied Bandwidth @ 315 MHz	F_{OBW315}	Measured @ -20 dBc, RBW = 1 kHz, SR = 1.2 kbps, t_{RAMP} = 256 us		6		kHz
Occupied Bandwidth @ 433.92 MHz	$F_{OBW433.92}$	Measured @ -20 dBc, RBW = 1 kHz, SR = 1.2 kbps, t_{RAMP} = 256 us		7		kHz

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[3]. The harmonics output is measured with the application shown as Figure 10.

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1.4 Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2110A can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

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2. Pin Descriptions

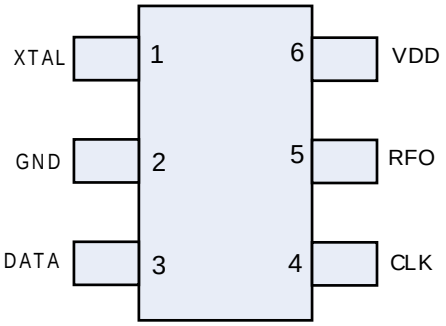

Figure 2. CMT2110A Pin Assignments

Table 6. CMT2110A Pin Descriptions

Pin Number	Name	I/O	Descriptions
1	XTAL	I	26 MHz single-ended crystal oscillator input or External 26 MHz reference clock input
2	GND	I	Ground
3	DATA	IO	Data input to be transmitted or Data pin to access the embedded EEPROM
4	CLK	I	Clock pin to access the embedded EEPROM
5	RFO	O	Power amplifier output
6	VDD	I	Power supply input

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3. Typical Performance Characteristics

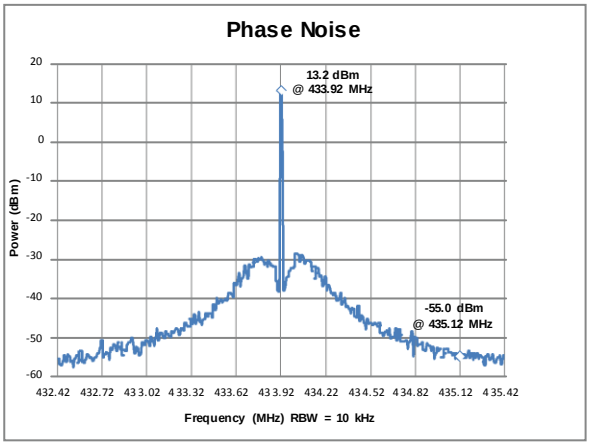

Figure 3. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

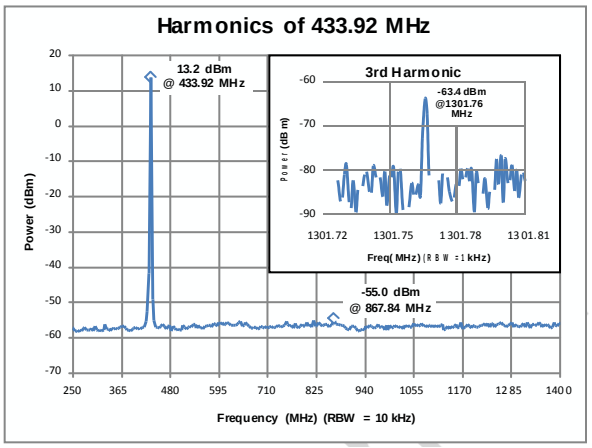

Figure 4. Harmonics of 433.92 MHz, P_{OUT} = +13 dBm

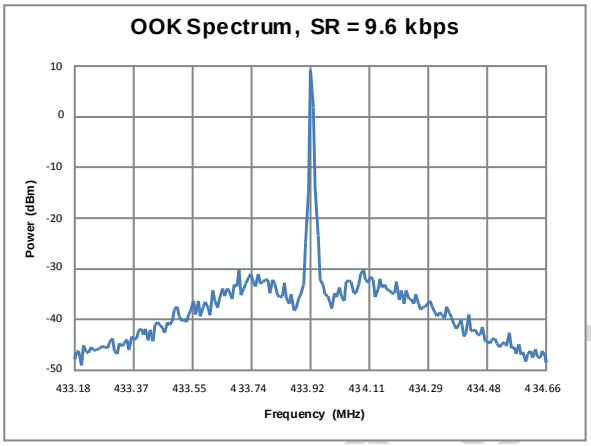

Figure 5. OOK Spectrum, SR = 9.6 kbps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

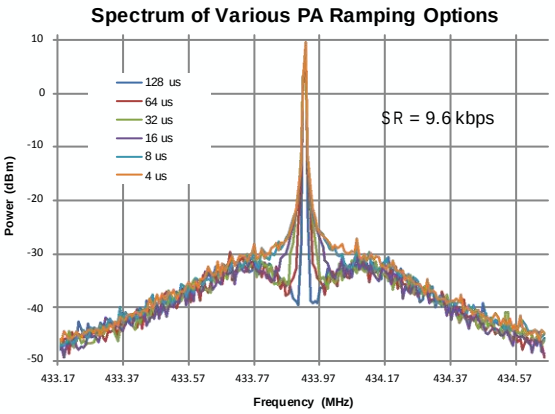

Figure 6. Spectrum of PA Ramping, SR = 9.6 kbps, P_{OUT} = +10 dBm

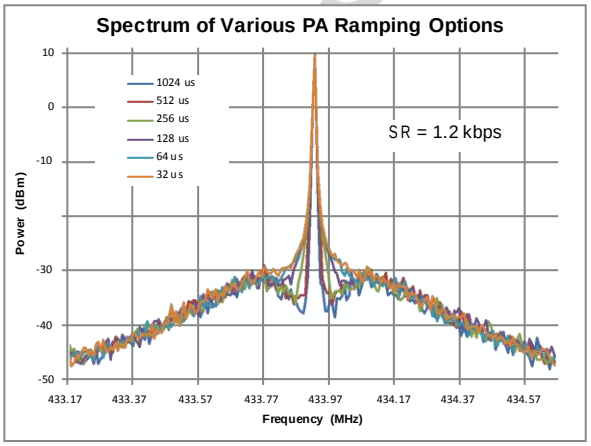

Figure 7. Spectrum of PA Ramping, SR = 1.2 kbps, P_{OUT} = +10 dBm

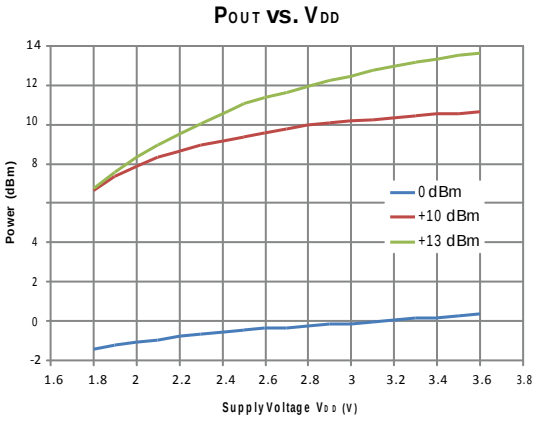

Figure 8. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Low-Cost Application Schematic

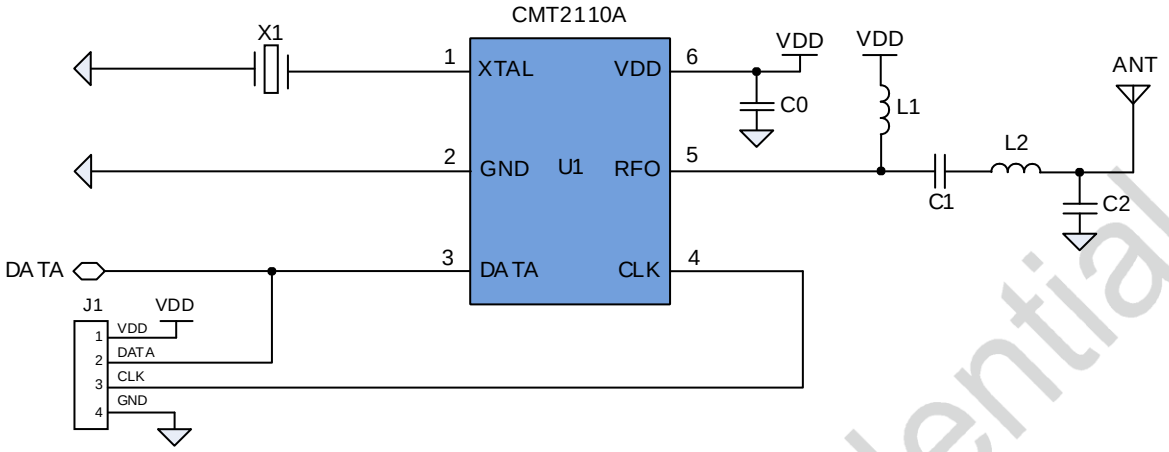

Figure 9. Low-Cost Application Schematic

Notes:

1. Connector J1 is a must for the CMT2110A EEPROM access during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to "AN101 CMT2110A Schematic and PCB Layout Design Guideline"
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2110A as possible for better filtering.
3. Table 7 shows the BOM of 433.92 MHz Low-Cost Application. For the BOM of 315 MHz application, please refer to "AN101 CMT2110A Schematic and PCB Layout Design Guideline".

Table 7. BOM of 433.92 MHz Low-Cost Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2110A, low-cost 240 – 480 MHz OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	27	nH	Murata LQG18

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4.2 FCC/ETSI Compliant Application Schematic

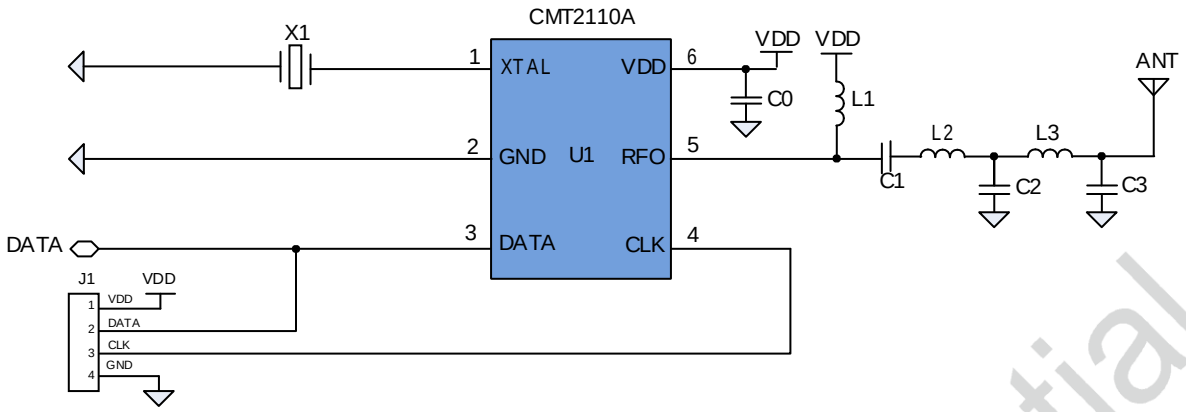

Figure 10. FCC/ETSI Compliant Application Schematic

Notes:

1. Connector J1 is a must for the CMT2110A EEPROM access during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to "AN101 CMT2110A Schematic and PCB Layout Design Guideline".
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2110A as possible for better filtering.
3. Table 8 shows the BOM of 433.92 MHz FCC/ETSI Compliant Application. For the BOM of 315 MHz application, please refer to "AN101 CMT2110A Schematic and PCB Layout Design Guideline".

Table 8. BOM of 433.92 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2110A, low-cost 240 – 480 MHz OOK transmitter			CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	36	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	18	nH	Murata LQG18

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5. Functional Descriptions

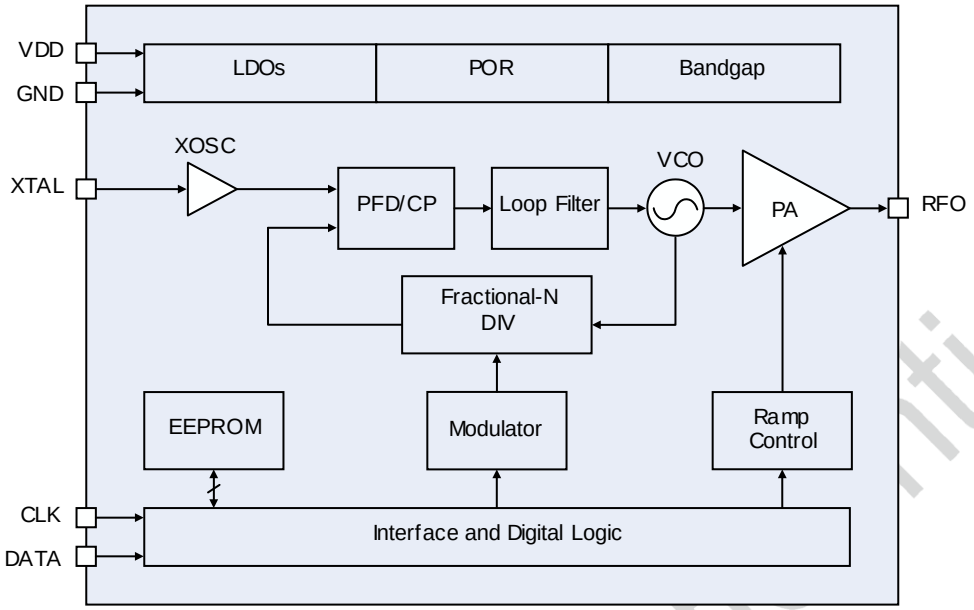

Figure 11. CMT2110A Functional Block Diagram

5.1 Overview

The CMT2110A is an ultra low-cost, highly flexible, high performance, single-chip OOK transmitter for various 240 to 480 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2110A is shown in Figure 11. The CMT2110A is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2110A requires only 1 wire for the external MCU or encoder to send in the data and control the transmission. The input data will be modulated and sent out by a highly efficient PA which output power can be configured from -10 to +13 dBm in 1 dB step size. RF Frequency, PA output power and other product features can be programmed into the embedded EEPROM by the RFPDK and USB Programmer. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 315/433.92 MHz are available for immediate demands with no need of EEPROM programming. The CMT2110A operates from 1.8 to 3.6 V so that it can finely work with most batteries to their useful power limits. It only consumes 12.4 mA when transmitting +10 dBm power under 3.3 V supply voltage.

5.2 Modulation, Frequency and Symbol Rate

The CMT2110A supports OOK modulation with the symbol rate up to 30 kbps. It continuously covers the frequency range from 240 to 480 MHz, including the license free ISM frequency band around 315 MHz and

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433.92 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz. See Table 9 for the modulation, frequency and symbol rate specifications.

Table 9. Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	OOK	-
Frequency	240 to 480	MHz
Frequency Resolution	198	Hz
Symbol Rate	0.5 to 30	kbps

5.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the CMT2110A in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See Figure 12 for the accessing of the EEPROM and Table 10 for the summary of all the configurable parameters of the CMT2110A in the RFPDK.

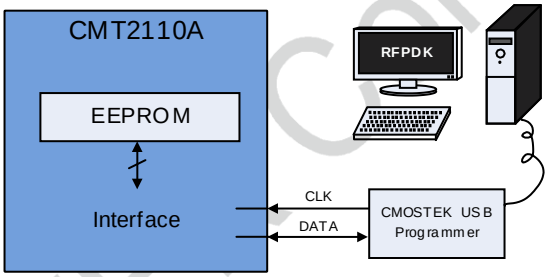

Figure 12. Accessing Embedded EEPROM

For more details of the CMOSTEK USB Programmer and the RFPDK, please refer to "AN103 CMT2110A/2210A One-Way RF Link Development Kits User's Guide". For the detail of CMT2110A configurations with the RFPDK, please refer to "AN102 CMT2110A Configuration Guideline".

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Table 10. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 480 MHz.	433.92 MHz	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dBm margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Cload	On-chip XOSC load capacitance options: from 10 to 22 pF.	15 pF	Basic Advanced
	PA Ramping	To control PA output power ramp up/down time, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 20 to 90 ms.	Data Pin Holding Low for 20 ms	Advanced

5.4 Power Amplifier

A highly efficient single-ended Power Amplifier (PA) is integrated in the CMT2110A to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN101 CMT2110A Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and RFPDK.

5.5 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2110A has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 13. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below:

$$SR_{Max} \le 0.5 * \left(\frac{1}{t_{RAMP}}\right)$$

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In which the PA ramping "rate" is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by:

$$t_{RAMP} \le 0.5 * (\frac{1}{SR_{MAX}})$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than "0.5 * ($1/SR_{Max}$)", it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to "AN102 CMT2110A Configuration Guideline".

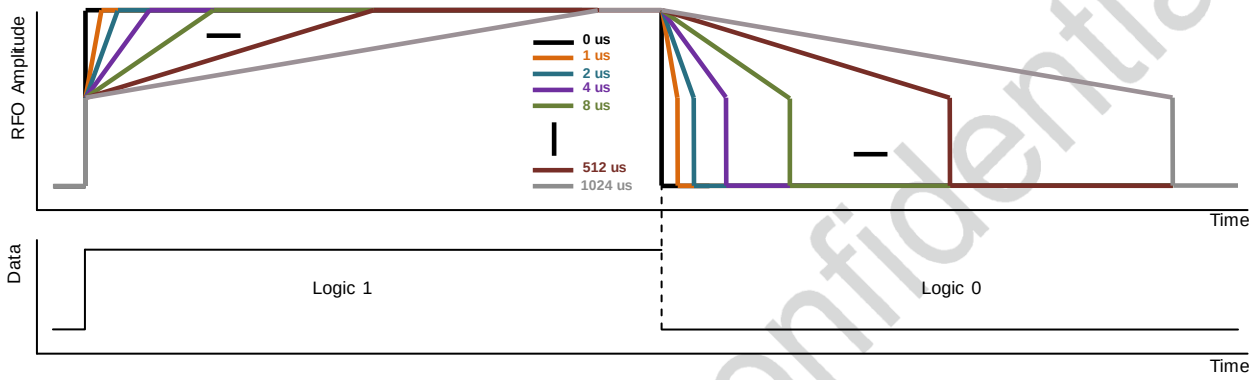

Figure 13. PA Ramping Time

5.6 Working States and Control Interface

The CMT2110A has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2110A is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized to 20 nA typically. The 1-wire interface is ready to sense a valid rising or falling edge on DATA pin to start a transmitting cycle.

XO-STARTUP

After the CMT2110A received the valid control signal, it will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table 11.

TUNE

The frequency synthesizer will tune the CMT2110A to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the incoming data only after the TUNE state is done, before that the incoming data (Don't Care shown in Figure 14 and 15) will not be transmitted.

TRANSMIT

The CMT2110A starts to modulate and transmit the data coming from the DATA pin. After the DATA pin is driven

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to low for the time t_{STOP} (can be configured from 20 to 90 ms in 10 ms step size through the RFPDK), the transmission will be ended and the CMT2110A will go back to the SLEEP state, waiting for the next transmitting cycle.

The transmission can be enabled by either “DATA Pin Rising Edge” or “DATA Pin Falling Edge”. See Table 11 and Figure 14, 15 for the timing requirement of each working state in the 2 different modes.

Table 11.Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	20		90	ms
Notes: [1]. This parameter is to a large degree crystal dependent [2]. Configurable from 20 to 90 ms in 10 ms step size					

5.6.1 Tx Enabled by DATA Pin Rising Edge

As shown in the Figure 14, once the CMT2110A detects a rising edge on the DATA pin, it goes into the XO-STARTUP state. The user has to pull the DATA pin high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the DATA pin. The logic state of the DATA pin is “don't’ care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission.

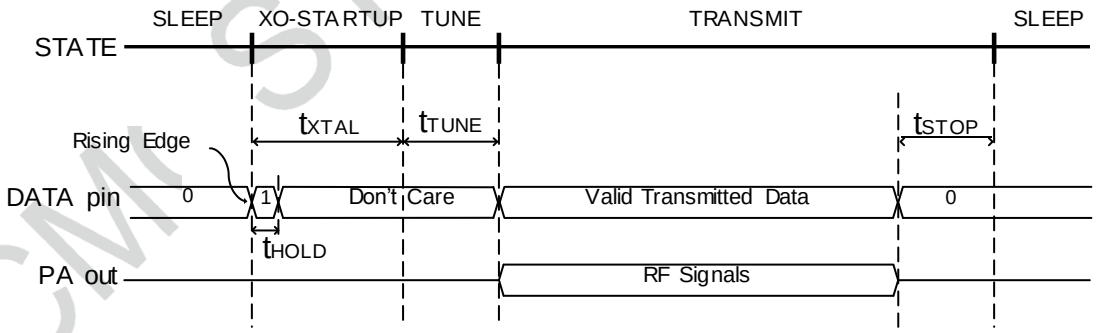

Figure 14. Transmission Enabled by DATA Pin Rising Edge

5.6.2 Tx Enabled by DATA Pin Falling Edge

As shown in the Figure 15, once the CMT2110A detects a falling edge on the DATA pin, it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the DATA pin needs to be pulled low. After the XO is settled, the CMT2110A goes to the TUNE state. The logic state of the DATA pin is “don't’ care” during the TUNE state. In the TRANSMIT state, PA sends out the input data after they are modulated. The user

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has to pull the DATA pin low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the DATA pin back to high.

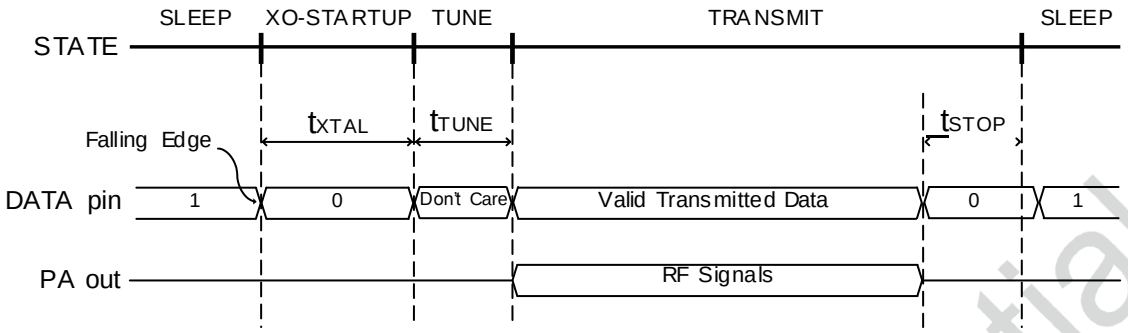

Figure 15. Transmission Enabled by DATA Pin Falling Edge

5.7 Crystal Oscillator and RCLK

The CMT2110A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 16 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2110A to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency. Please refer to "AN103 CMT2110A/2210A One-Way RF Link Development Kits User's Guide" for the method of choosing the right value of C_L.

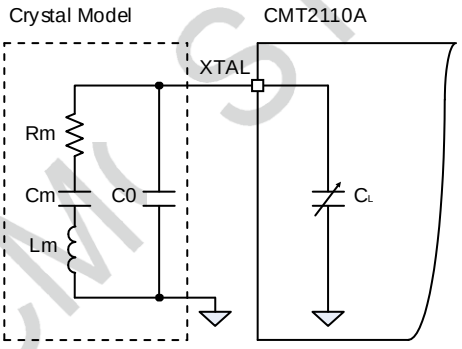

Figure 16. XTAL Circuitry and Crystal Model

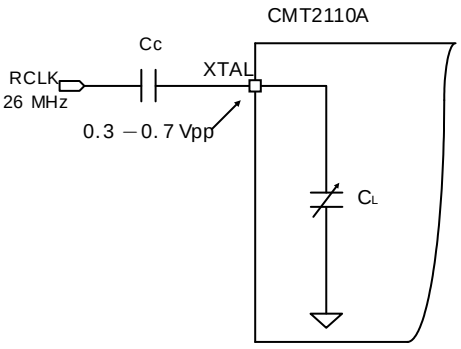

Figure 17. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2110A by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 17 for the RCLK circuitry.

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6. Ordering Information

Table 12. CMT2110A Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2110A-ESR[1]	Low-Cost 240-480 MHz OOK Transmitter	SOT23-6	Tape & Reel	1.8 to 3.6V, -40 to 85℃	3,000
CMT2110A-ESR3[1]	Low-Cost 315 MHz OOK Transmitter	SOT23-6	Tape & Reel	1.8 to 3.6V, -40 to 85℃	3,000
CMT2110A-ESR4[1]	Low-Cost 433.92 MHz OOK Transmitter	SOT23-6	Tape & Reel	1.8 to 3.6V, -40 to 85℃	3,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85℃.

"S" stands for the package type of SOT23-6.

"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 3,000 pieces.

"3" in the suffix stands for in stock product of 315 MHz with no need of EEPROM programming.

"4" in the suffix stands for in stock product of 433.92 MHz with no need of EEPROM programming.

If the CMT2110A-ESR3/4cannot meet the application requirements, the user can order the CMT2110A-ESR for self-customizing with the RFPDK.

Default Configurations	CMT2110A-ESR3	CMT2110A-ESR4	CMT2110A-ESR
Frequency	315.00 MHz	433.92 MHz	Random
Others	Refer to the default values in Table 10 of Page 14		

Visit www.hoperf.com to know more about the product and product line.

Contact sales@hoperf.com or your local sales representatives for more information.

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7. Package Outline

The 6-pin SOT23-6 illustrates the package details for the CMT2110A. Table 13 lists the values for the dimensions shown in the illustration.

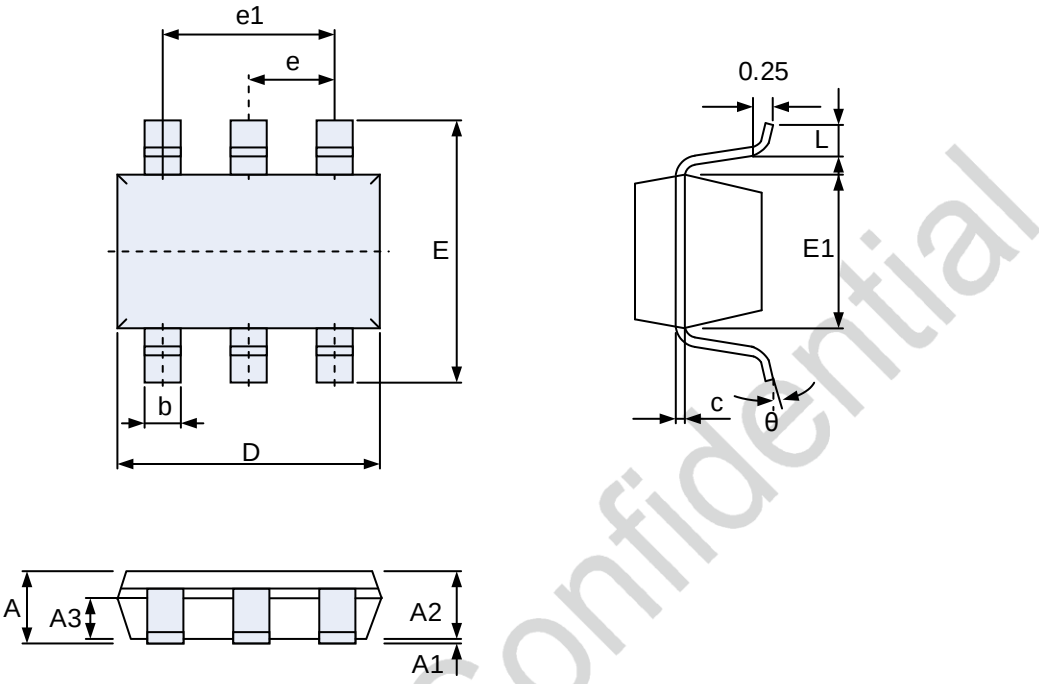

Figure 18. 6-Pin SOT23-6

Table 13. 6-Pin SOT23-6 Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	—	—	1.35
A1	0.04	—	0.15
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
b	0.38	—	0.48
C	0.08	—	0.20
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ	0	—	8°

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8. Top Marking

8.1 CMT2110A Top Marking

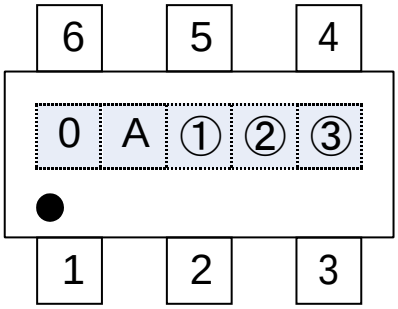

Figure 19. CMT2110A Top Marking

Table 14. CMT2110A Top Marking Explanation

Top Mark :	0A①②③
Mark Method :	Laser
Font Size :	0.6 mm, right-justified
1st letter:	0, represents CMT2110
2nd letter:	A: represents revision A
3rd – 5th letter:	①②③: Internal reference for data code tracking, assigned by the assembly house

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9. Other Documentations

Table 15. Other Documentations for CMT2110A

Brief	Name	Descriptions
AN101	CMT2110A Schematic and PCB Layout Design Guideline	Details of CMT2110A PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN102	CMT2110A Configuration Guideline	Details of configuring CMT2110A features on the RFPDK.
AN103	CMT2110A/2210A One-Way RF Link Development Kits User's Guide	User's Guides for CMT2110A/2210A Development Kits, including Evaluation Board and Evaluation Module, CMOSTEK USB Programmer and RFPDK.

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10. Document Change List

Table 16. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.7		Initial released version	2014-03-04
0.8	0 1 3 4 5	Add Ordering Information in first page Update Table 4 Update the title of Figure7/8 Update the BOM of Typical Application Schematics Update Section 5.3 Embedded EEPROM and RFPDK Add Section 5.5 PA Ramping	2014-04-05
0.85	1 3	Update Table 4 Update Figure 3	2014-04-08
0.9	0 5 6	Update ordering Information in first page Update Description Update 5.3, add Table 10 Update chapter 6. Ordering information	2014-06-14
1.0	-	-	2014-06-30

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