

DMOS Full-Bridge Motor Driver

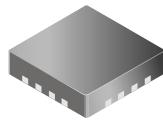
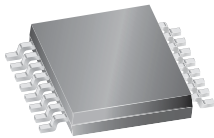
Features and Benefits

- Low $R_{DS(on)}$ outputs
- Overcurrent protection
- Motor lead short-to-supply protection
- Short-to-ground protection
- Sleep function
- Synchronous rectification
- Diagnostic output
- Internal undervoltage lockout (UVLO)
- Crossover-current protection

Packages:

Package LP, 16 pin TSSOP with Exposed Thermal Pad

Package EU, 16 pin QFN with Exposed Thermal Pad



Approximate Scale 1:1



Description

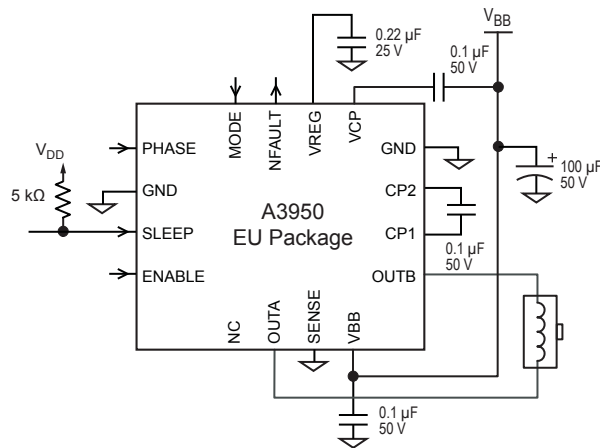
Designed for PWM (pulse width modulated) control of DC motors, the A3950 is capable of peak output currents to ± 2.8 A and operating voltages to 36 V.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

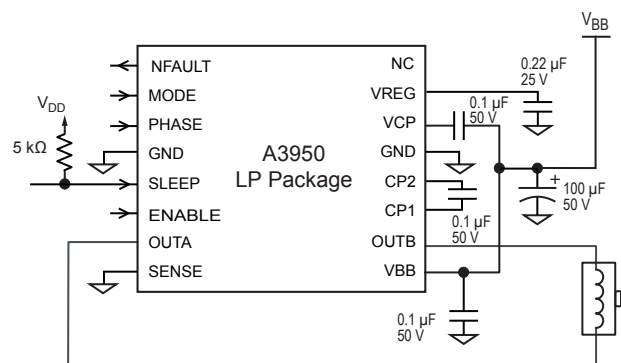
Internal circuit protection includes motor lead short-to-supply/short-to-ground, thermal shutdown with hysteresis, undervoltage monitoring of V_{BB} and V_{CP} , and crossover-current protection.

The A3950 is supplied in a thin profile (< 1.2 mm overall height) 16 pin TSSOP package (LP), and a very thin (0.75 mm nominal height) QFN package. Both packages provide an exposed pad for enhanced thermal dissipation, and are lead (Pb) free with 100% matte tin leadframe plating.

Typical Application Diagrams



Package EU



Package LP

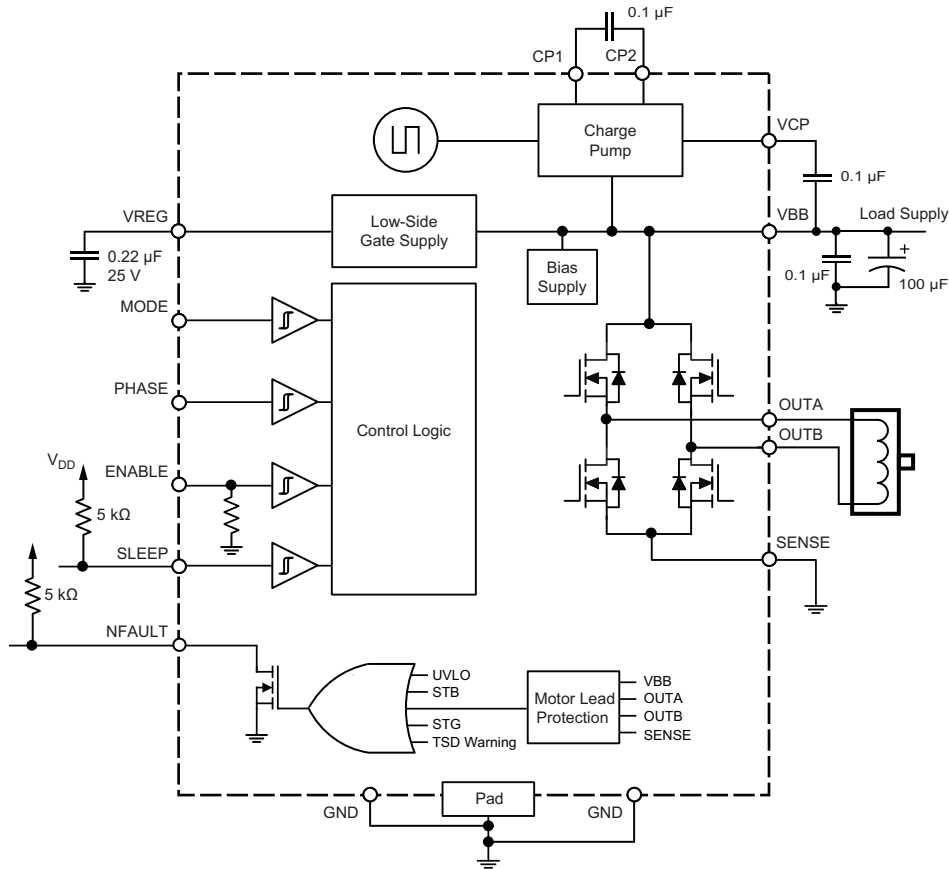
Selection Guide

Part Number	Packing	Package
A3950SLPTR-T	13 in. reel, 4000 pieces/reel	16 pin TSSOP with exposed thermal pad
A3950SEUTR-T	7 in. reel, 1500 pieces/reel	16 pin QFN with exposed thermal pad

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		36	V
Output Current	I_{OUT}		2.8	A
Sense Voltage	V_{SENSE}		±500	mV
VBB to OUTx			36	V
OUTx to SENSE			36	V
Logic Input Voltage	V_{IN}		-0.3 to 7	V
Operating Ambient Temperature	T_A	Range S	-20 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		-40 to 125	°C

Functional Block Diagram



Terminal List Table

Name	Number		Description
	EU	LP	
NFAULT	15	1	Fault output, open drain
MODE	16	2	Logic input
PHASE	1	3	Logic input for direction control
GND	2, 12	4, 13	Ground
SLEEP	3	5	Logic input
ENABLE	4	6	Logic input
OUTA	6	7	DMOS full-bridge output A
SENSE	7	8	Power return
VBB	8	9	Load supply voltage
OUTB	9	10	DMOS full-bridge output B
CP1	10	11	Charge pump capacitor terminal
CP2	11	12	Charge pump capacitor terminal
VCP	13	14	Reservoir capacitor terminal
VREG	14	15	Regulator decoupling terminal
NC	5	16	No connection
Pad	-	-	Exposed pad for thermal dissipation connect to GND pins

ELECTRICAL CHARACTERISTICS at T_J = 25°C, V_{BB} = 8 to 36 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Motor Supply Current	I _{BB}	f _{PWM} < 50 kHz	–	6	8.5	mA
		Charge pump on, outputs disabled	–	3	4.5	mA
		Sleep mode	–	–	10	µA
PHASE, ENABLE, MODE Input Voltage	V _{IH}		2.0	–	–	V
	V _{IL}		–	–	0.8	V
SLEEP Input Voltage	V _{IH}		2.7	–	–	V
	V _{IL}		–	–	0.8	V
PHASE, MODE Input Current ¹	I _{IH}	V _{IN} = 2.0 V	–	<1.0	20	µA
	I _{IL}	V _{IN} = 0.8 V	–20	<–2.0	20	µA
ENABLE Input Current	I _{IH}	V _{IN} = 2.0 V	–	40	100	µA
	I _{IL}	V _{IN} = 0.8 V	–	16	40	µA
SLEEP Input Current	I _{IH}	V _{IN} = 2.7 V	–	27	50	µA
	I _{IL}	V _{IN} = 0.8 V	–	<1	10	µA
NFAULT Output Voltage	V _{OL}	I _{sink} = 1.0 mA	–	–	0.4	V
Input Hysteresis, except SLEEP	V _{IHys}		100	150	250	mV
Output On Resistance	R _{DS(on)}	Source driver, I _{OUT} = –2.8 A, T _J =25°C	–	0.35	0.48	Ω
		Source driver, I _{OUT} = –2.8 A, T _J =125°C	–	0.55	0.8	Ω
		Sink driver, I _{OUT} = 2.8 A, T _J =25°C	–	0.3	0.43	Ω
		Sink driver, I _{OUT} = 2.8 A, T _J =125°C	–	0.45	0.7	Ω
Body Diode Forward Voltage ¹	V _f	Source diode, I _f = –2.8 A	–	–	1.4	V
		Sink diode, I _f = 2.8 A	–	–	1.4	V
Propagation Delay Time	t _{pd}	PWM, change to source or sink ON	–	600	–	ns
		PWM, change to source or sink OFF	–	100	–	ns
Crossover Delay	t _{COD}		–	500	–	ns
Protection Circuitry						
UVLO Threshold	V _{UV}	V _{BB} increasing	–	6.5	–	V
UVLO Hysteresis	V _{UVHys}		–	250	–	mV
Overcurrent Threshold ²	I _{OCP}		3	–	–	A
Overcurrent Protection Period	t _{OCP}		–	1.2	–	ms
Thermal Warning Temperature	T _{JW}	Temperature increasing	–	160	–	°C
Thermal Warning Hysteresis	T _{JWHys}	Recovery = T _{JW} – T _{JWHys}	–	15	–	°C
Thermal Shutdown Temperature	T _{JTSD}	Temperature increasing	–	175	–	°C
Thermal Shutdown Hysteresis	T _{JTSDHys}	Recovery = T _{JTSD} – T _{JTSDHys}	–	15	–	°C

¹For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

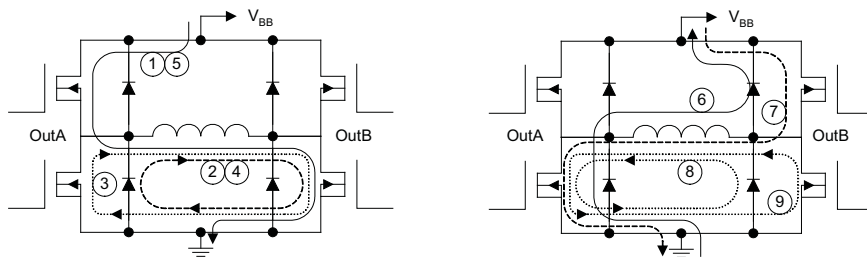
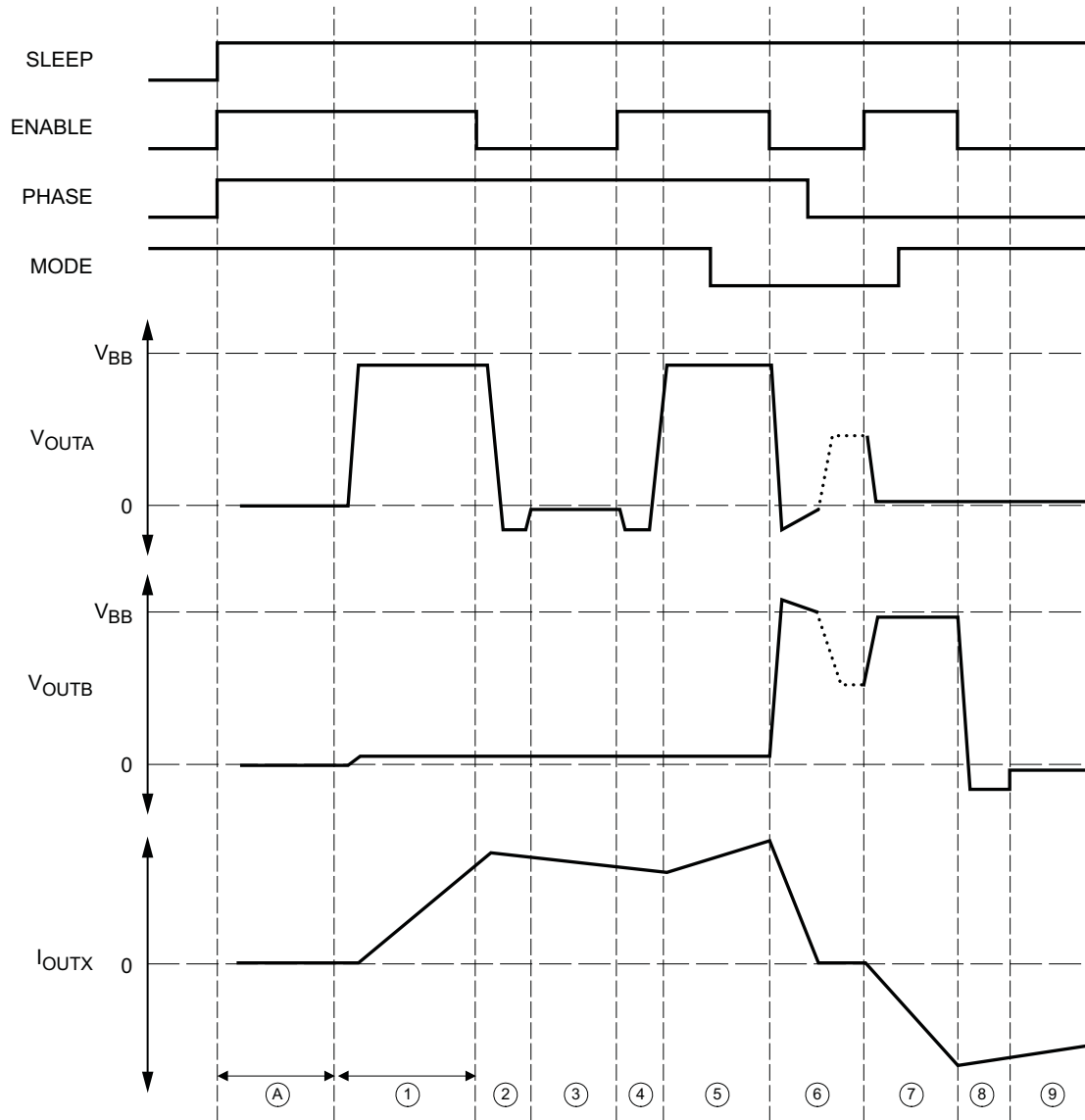
²Overcurrent protection is tested at 25°C in a restricted range and guaranteed by characterization.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	R _{θJA}	Preliminary: EU package, 4-layer PCB based on JEDEC standard	30	°C/W
		LP package, 4-layer PCB based on JEDEC standard	34	°C/W
		LP package, 2-layer PCB with 3.8 in. ² copper both sides, connected by thermal vias	43	°C/W

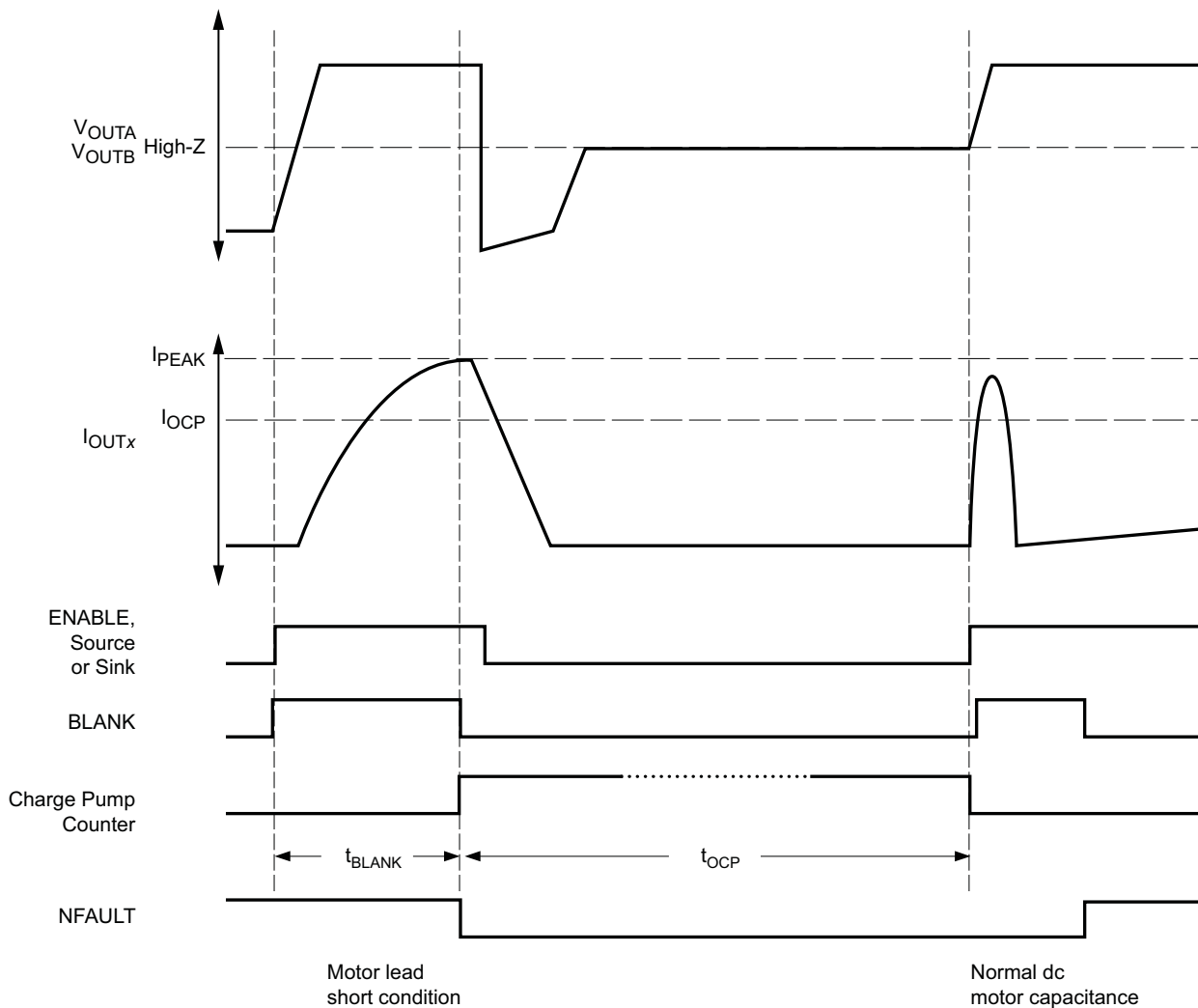
*Additional thermal data available on the Allegro Web site.

Timing Diagram: PWM Control



(A) Charge pump and VREG power-on delay ($\approx 200 \mu\text{s}$)

Timing Diagram: Overcurrent Control



Functional Description

Device Operation. The A3950 is designed to operate one DC motor. The output drivers are all low $R_{DS(on)}$ N-channel DMOS drivers that feature internal synchronous rectification to reduce power dissipation. PHASE and ENABLE inputs allow two-wire control with an additional MODE pin for the brake function. A low current Sleep mode is provided to minimize power consumption when the driver is disabled. In addition, the driver also has built-in protection from short-to-ground, short-to-battery, and shorted load events.

Logic Inputs. If logic inputs are pulled up to V_{DD} , it is good practice to use a high value pull-up resistor in order to limit current to the logic inputs should an overvoltage event occur. Logic inputs include: SLEEP, MODE, PHASE, and ENABLE. The voltage on any logic input cannot exceed the specified maximum of 7 V.

VREG. This supply voltage is used to run the sink-side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The VREG pin should be decoupled with a 0.22 μ F capacitor to ground.

Charge Pump. The charge pump is used to generate a supply above V_{BB} to drive the source-side DMOS gates. A 0.1 μ F ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 μ F ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on VCP or VREG, the outputs of

the device are disabled until the fault condition is removed. At power-on the UVLO circuit disables the drivers.

Sleep Mode. Control input SLEEP is used to minimize power consumption when the A3950 is not in use. This disables much of the internal circuitry, including the regulator and charge pump. A logic low setting puts the device into Sleep mode, and a logic high setting allows normal operation. After coming out of Sleep mode, provide a 1 ms interval before applying PWM signals, to allow the charge pump to stabilize.

MODE. Control input MODE is used to toggle between fast decay mode and slow decay mode. A logic high puts the device in slow decay mode. Synchronous rectification is always enabled.

Braking. The braking function is implemented by driving the device in slow decay mode via the MODE setting and applying an enable chop command. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by V_{BEMF}/R_L . Care should be taken to insure that the maximum ratings of the device are not exceeded in worse case braking situations: high speed and high-inertia loads.

Diagnostic Output. The NFAULT pin signals a problem with the chip via an open drain output. A motor fault, undervoltage condition, or $T_j > 160^\circ\text{C}$ will drive the pin active low. This output is not valid when SLEEP puts the device into minimum power dissipation mode.

TSD. Two die temperature monitors are integrated on the chip. As die temperature increases towards the maximum, a thermal warning signal will be triggered at 160°C . This fault drives the

Control Logic Table¹

Pin						Function
PHASE	ENABLE	MODE	SLEEP	OUTA	OUTB	
1	1	X	1	H	L	Forward
0	1	X	1	L	H	Reverse
X	0	1	1	L	L	Brake (slow decay)
1	0	0	1	L	H	Fast Decay Synchronous Rectification ²
0	0	0	1	H	L	Fast Decay Synchronous Rectification ²
X	X	X	0	Z	Z	Sleep Mode

¹X indicates "don't care," Z indicates high impedance.

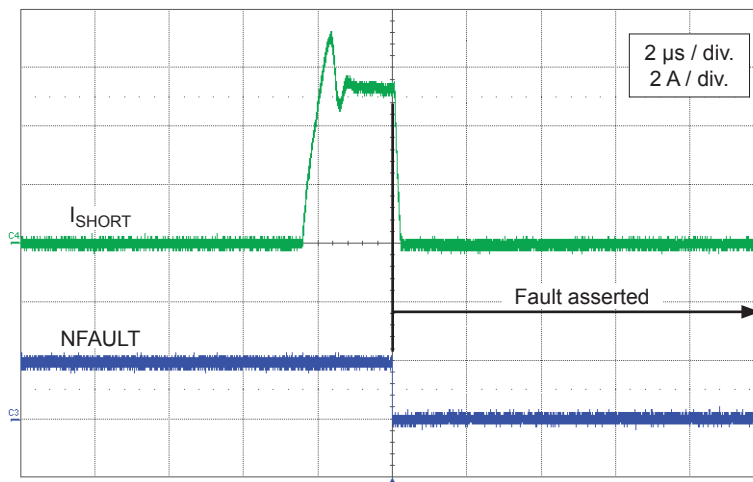
²To prevent reversal of current during fast decay synchronous rectification, outputs go to the high impedance state as the current approaches 0 A.

NFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs will be disabled until the internal temperature falls below a hysteresis of 15°C.

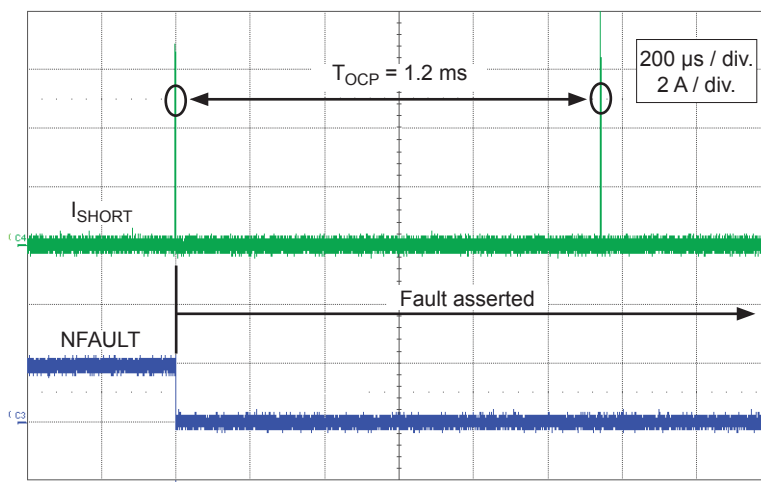
Overcurrent Protection. Referring to the figures below, the voltage on the output pins relative to supply are monitored to ensure that the motor lead is not shorted to supply or ground.

If a short is detected, the full-bridge outputs are turned off, flag NFAULT is driven low, and a 1.2 ms fault timer is started.

After this 1.2 ms period, t_{OCP} , the device will then be allowed to follow the input commands and another turn-on is attempted. If there is still a fault condition, the cycle repeats. If, after t_{OCP} expires, it is determined that the short condition is not present, the NFAULT pin is released and normal operation resumes.



Shorted load condition, output current waveform is shown along with the NFAULT output.



Shorted load condition illustrating repetitive cycles with a 1.2 ms delay.

Applications Information

Power Dissipation. First order approximation of power dissipation in the A3950 can be calculated by first examining the power dissipation in the full-bridge during each of the operation modes. The A3950 features synchronous rectification, a feature that effectively shorts out the body diode by turning on the low $R_{DS(on)}$ DMOS driver during the decay cycle. This significantly reduces power dissipation in the full-bridge. In order to prevent shoot-through, where both

source and sink driver are on at the same time, the A3950 implements a 500 ns typical crossover delay time. For this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. This does affect power dissipation and should be considered in high current, high ambient temperature applications. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

Drive Current. This current path is through source DMOS driver, motor winding, and sink DMOS driver. Power dissipation is I^2R losses in one source and one sink DMOS driver, as shown in the following equation:

$$P_D = I^2 (R_{DS(on)Source} + R_{DS(on)Sink}) \tag{1}$$

Fast Decay with Synchronous Rectification. This decay mode is equivalent to a phase change where the opposite drivers are switched on. When in fast decay, the motor current is not allowed to go negative (direction change). Instead, as the current approaches zero, the drivers turn off. The power calculation is the same as the drive current calculation, equation 1:

Slow Decay SR (Brake Mode). In this decay mode, both sink drivers turn on, allowing the current to circulate through the sink drivers and the load. Power dissipation is I^2R losses in the two sink DMOS drivers:

$$P_D = I^2 (2 \times R_{DS(on)Sink}) \tag{2}$$

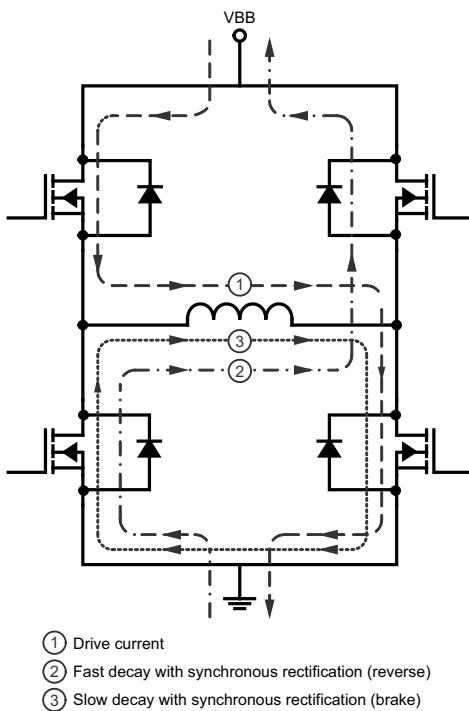


Figure 1. Current Decay Patterns

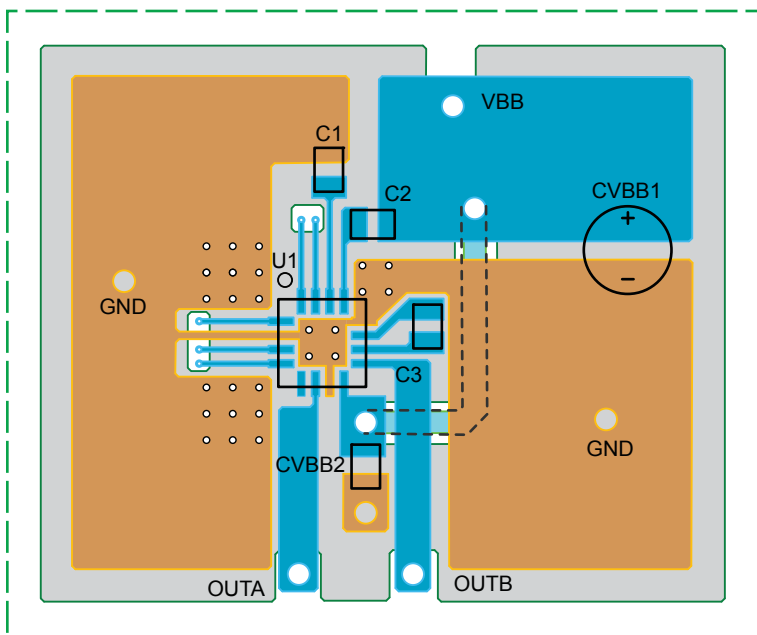
SENSE Pin. A low value resistor can be placed between the SENSE pin and ground for current sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

When selecting a value for the sense resistor be sure not to exceed the maximum voltage on the SENSE pin of ± 500 mV.

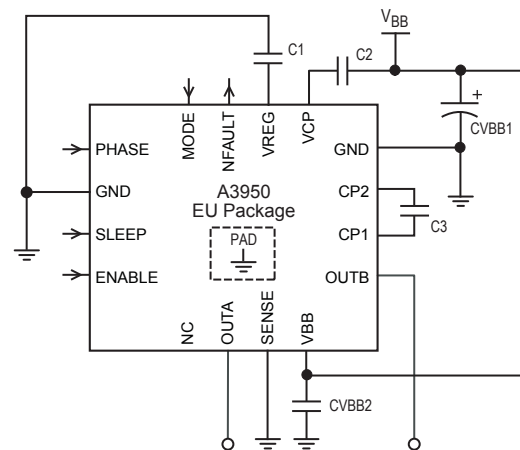
Ground. A star ground should be located as close to the A3950 as possible. The copper ground plane directly under the exposed thermal pad makes a good location for the star ground point. The exposed pad can be connected to ground for this purpose.

Layout. The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the A3950 must be soldered directly onto the board. On the underside of the A3950 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

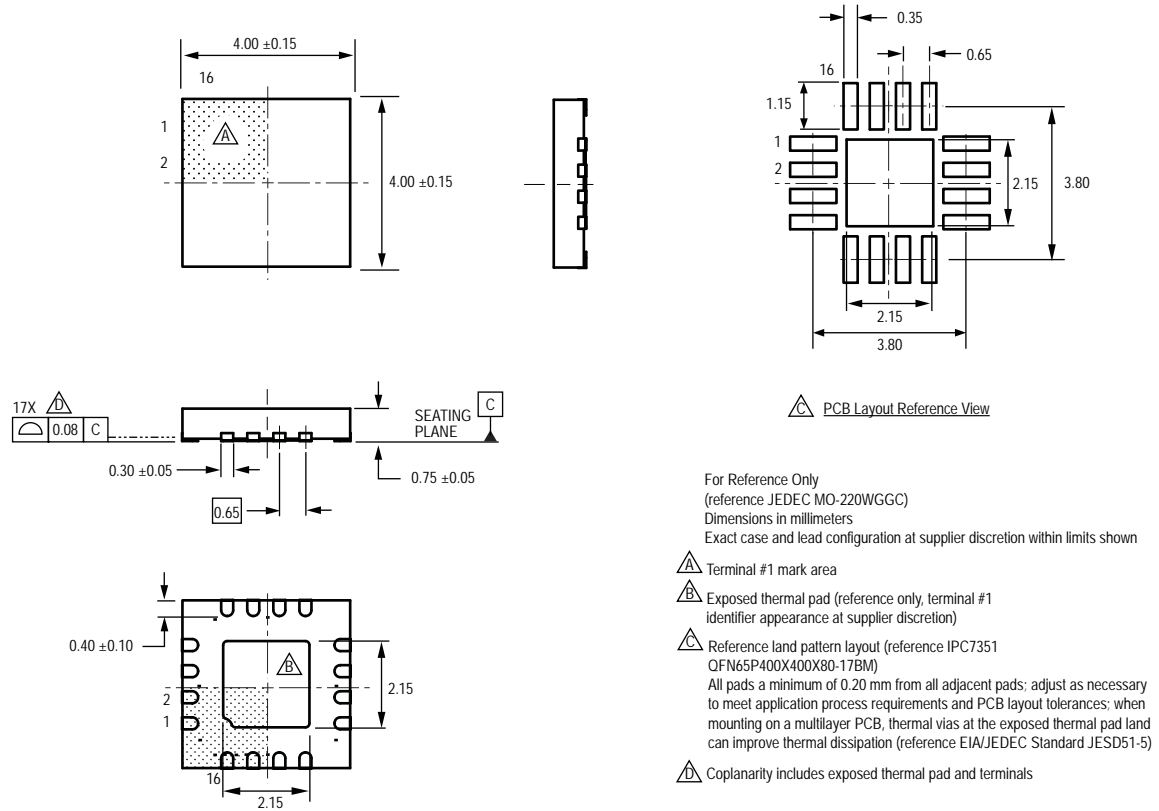
The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 μ F) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2, should be as close to the pins of the device as possible, in order to minimize lead inductance.



EU package shown



EU Package, 16 Pin QFN with Exposed Thermal Pad

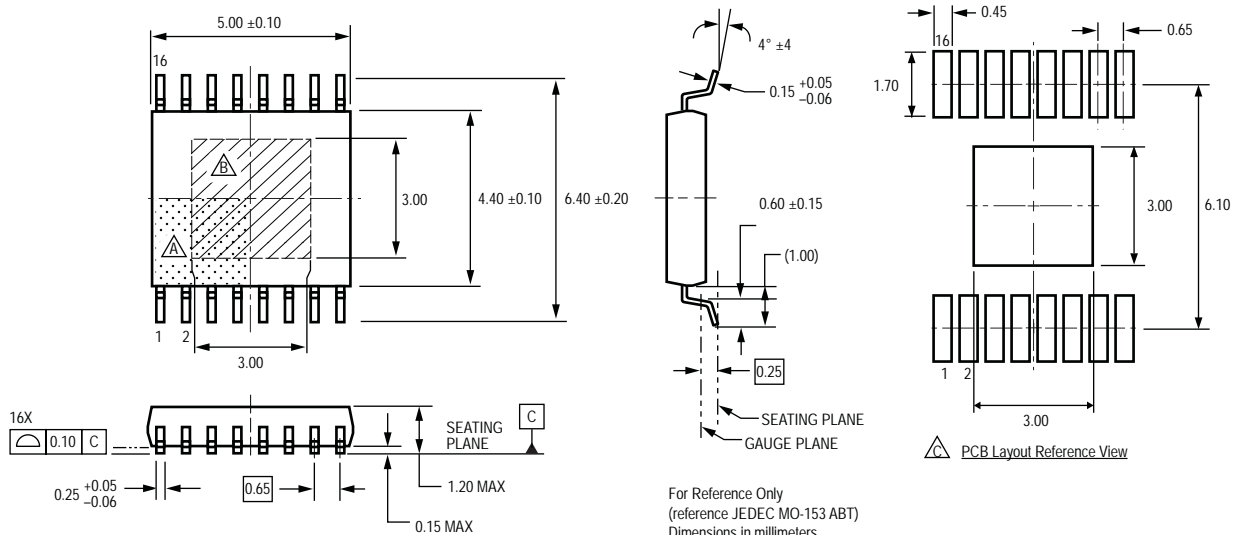


PCB Layout Reference View

For Reference Only
 (reference JEDEC MO-220WGGC)
 Dimensions in millimeters
 Exact case and lead configuration at supplier discretion within limits shown

- Terminal #1 mark area
- Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- Reference land pattern layout (reference IPC7351 QFN65P400X400X80-17BM)
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- Coplanarity includes exposed thermal pad and terminals

LP Package, 16 Pin TSSOP with Exposed Thermal Pad



- For Reference Only
 (reference JEDEC MO-153 ABT)
 Dimensions in millimeters
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
 Exact case and lead configuration at supplier discretion within limits shown
- △ Terminal #1 mark area
 - △ Exposed thermal pad (bottom surface)
 - △ Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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