iW3612

AC/DC Digital Power Controller for Dimmable LED Drivers

1.0 Features

- Isolated AC/DC offline 100 V_{AC} / 230 V_{AC} LED driver
- Line frequency ranges from 45 Hz to 66 Hz
- Intelligent wall dimmer detection
  - Leading-edge dimmer
  - Trailing-edge dimmer
  - No-dimmer detected
  - Unsupported dimmer
- Hybrid dimming scheme
- Wide dimming range from 1% up to 100%
- No visible flicker
- Resonant control to achieve high efficiency, 85% without dimmer
- Temperature compensated LED current
- Small size design
  - Small size input bulk capacitor
  - Small size output capacitor
  - Small transformer
- Primary-side sensing eliminates the need for opto-isolator feedback and simplifies design
- Tight LED current regulation ± 5%
- Fast start-up, typically 10 µA start-up current
- Hot-plug LED module support
- Multiple protection features:
  - LED open circuit protection
  - Single-fault protection
  - Over-current protection
  - LED short circuit protection
  - Current sense resistor short circuit protection
  - Over-temperature protection
  - Input over-voltage protection
- Up to 25 W output power

2.0 Description

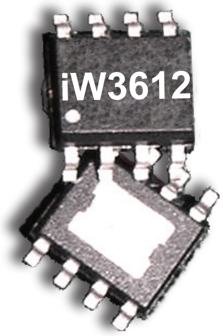
The iW3612 is a high performance AC/DC offline power supply controller for dimmable LED luminaires, which uses advanced digital control technology to detect the dimmer type and phase. The dimmer conduction phase controls the LED brightness. The LED brightness is modulated by PWM-dimming. iW3612's unique digital control technology eliminates visible flicker.

iW3612 can operate with all dimmer schemes including: leading-edge dimmer, trailing-edge dimmer, as well as other dimmer configurations such as R-type, R-C type or R-L type. When a dimmer is not present, the controller can automatically detect that there is no dimmer.

iW3612 operates in quasi-resonant mode to provide high efficiency. The iW3612 provides a number of key built-in features. The iW3612 uses iWatt's advanced primary-side sensing technology to achieve excellent line and load regulation without secondary feedback circuitry. In addition, iW3612's pulse-by-pulse waveform analysis technology allows accurate LED current regulation. The iW3612 maintains stability over all operating conditions without the need for loop compensation components. Therefore, the iW3612 minimizes external component count, simplifies EMI design and lowers overall bill of materials cost.

3.0 Applications

- Dimmable LED luminaires
- Optimized for 8 W - 25 W output power



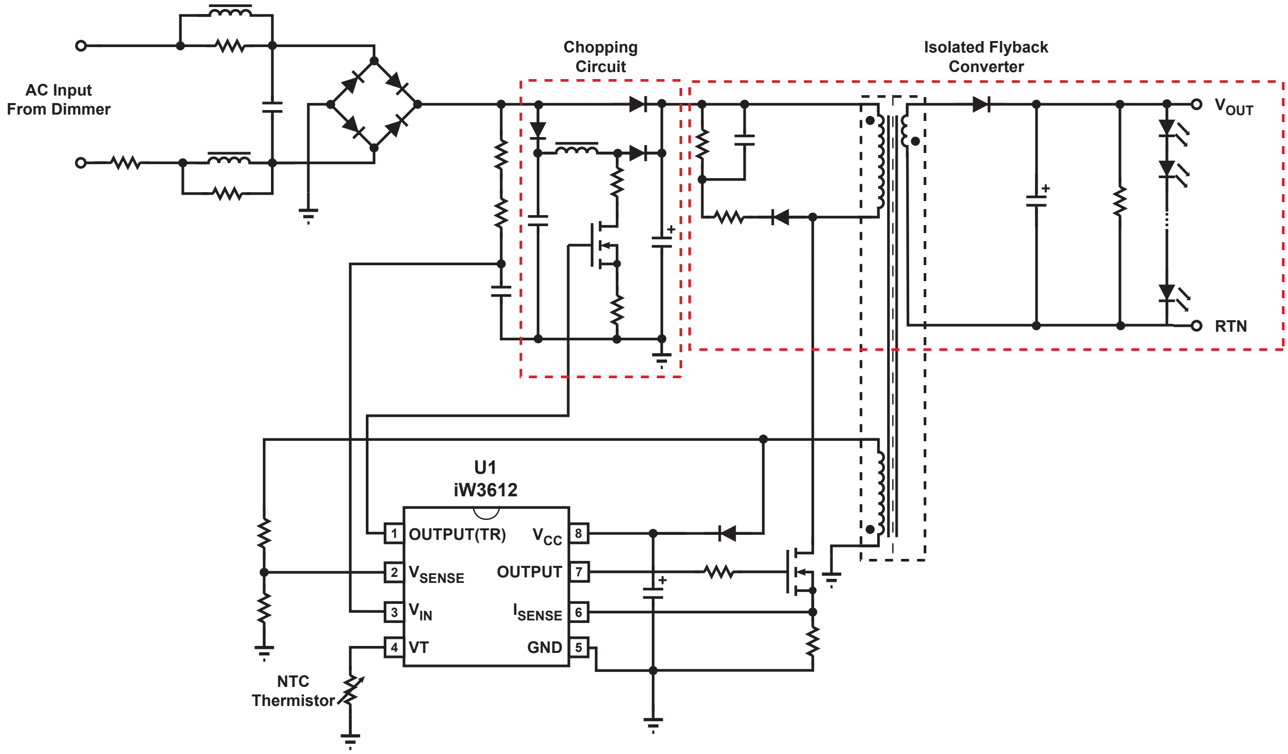
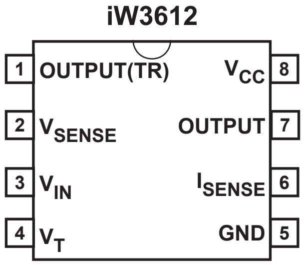


Figure 3.1 : Typical Application Circuit

4.0 Pinout Description



Pin #	Name	Type	Pin Description
1	OUTPUT(TR)	Output	Gate drive for chopping MOSFET switch
2	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary side regulation and ZVS)
3	V_{IN}	Analog Input	Rectified AC line voltage sense
4	V_T	Analog Input	External power limit and shutdown control
5	GND	Ground	Ground
6	I_{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit)
7	OUTPUT	Output	Gate drive for main MOSFET switch
8	V_{CC}	Power Input	Power supply for control logic and voltage sense for power-on reset circuitry

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18	V
DC supply current at V_{CC} pin	I_{CC}	20	mA
OUTPUT (pin 7)		-0.3 to 18	V
OUTPUT(TR) (pin 1)		-0.3 to 18	V
V_{SENSE} input (pin 2, $I_{Vsense} \leq 10$ mA)		-0.7 to 4.0	V
V_{IN} input (pin 3)		-0.3 to 18	V
I_{SENSE} input (pin 6)		-0.3 to 4.0	V
V_T input (pin 4)		-0.3 to 4.0	V
Power dissipation at $T_A \leq 25$°C	P_D	526	mW
Maximum junction temperature	$T_{J\,MAX}$	150	°C
Storage temperature	T_{STG}	–65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	°C
Thermal Resistance Junction-to-PCB Board Surface Temperature	ψ_{JB} (Note 1)	70	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-Up test per JEDEC 78		±100	mA

Notes:

Note 1. ψ_{JB} [Psi Junction to Board] provides an estimation of the die junction temperature relative to the PCB [**B**oard] surface temperature. This data is measured at the ground pin (pin 5) without using any thermal adhesives. See Section 9.13 for more information.

6.0 Electrical Characteristics

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} SECTION (Pin 3)						
Start-up current	I_{INST}	V_{IN} = 10 V, C_{VCC} = 10 µF		10	15	µA
Input impedance	Z_{IN}	T_A = 25°C		2.5		kΩ
V_{IN} Range	V_{IN}		0		1.8	V
V_{SENSE} SECTION (Pin 2)						
Input leakage current	$I_{IN(Vsense)}$	V_{SENSE} = 2 V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A = 25°C, negative edge	1.523	1.538	1.553	V
Output OVP threshold	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge	1.65	1.7	1.75	V
OUTPUT SECTION (Pin 7)						
Output low level ON-resistance	$R_{DS(ON)LO}$	I_{SINK} = 5 mA		30		Ω
Output high level ON-resistance	$R_{DS(ON)HI}$	I_{SOURCE} = 5 mA		50		Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330 pF 10% to 90%		50		ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330 pF 90% to 10%		30		ns
Maximum switching frequency (Note 3)	$f_{SW(MAX)}$			200		kHz
V_{CC} SECTION (Pin 8)						
Maximum operating voltage	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	11	12	13	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	7	7.5	8	V
Operating current	I_{CCQ}	C_L = 330 pF, V_{SENSE} = 1.5 V		4.1	4.7	mA
Zener diode clamp voltage	$V_{Z(CLAMP)}$	T_A = 25°C, I_Z = 5 mA	18.5	19	20.5	V

6.0 Electrical Characteristics (cont.)

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I_{SENSE} SECTION (Pin 6)						
Over-current limit threshold	V_{OCP}		1.83	1.89	1.95	V
Isense short protection reference	V_{RSNS}			0.16		V
CC regulation threshold limit (Note 4)	V_{REG-TH}			1.8		V
V_T SECTION (Pin 4)						
Power limit high threshold (Note 4)	$V_{P-LIM(HI)}$			0.56		V
Power limit low threshold (Note 4)	$V_{P-LIM(LO)}$			0.44		V
Shutdown threshold (Note 4)	V_{SH-TH}			0.22		V
Input leakage current	$I_{IN(VT)}$	V_T = 1.0 V			1	μA
Pull up current source	I_{VT}		90	100	110	μA
OUTPUT(TR) SECTION (Pin 1)						
Output low level ON-resistance	$R_{DS-TR(ON)LO}$	I_{SINK} = 5 mA		100		Ω
Output high level ON-resistance	$R_{DS-TR(ON)HI}$	I_{SOURCE} = 5 mA		200		Ω

Notes:

Note 1. Adjust V_{CC} above the start-up threshold before setting at 12 V.

Note 2. These parameters are not 100% tested, guaranteed by design and characterization.

Note 3. Operating frequency varies based on the line and load conditions, see Theory of Operation for more details.

Note 4. These parameters refer to digital preset values, and are not 100% tested.

7.0 Typical Performance Characteristics

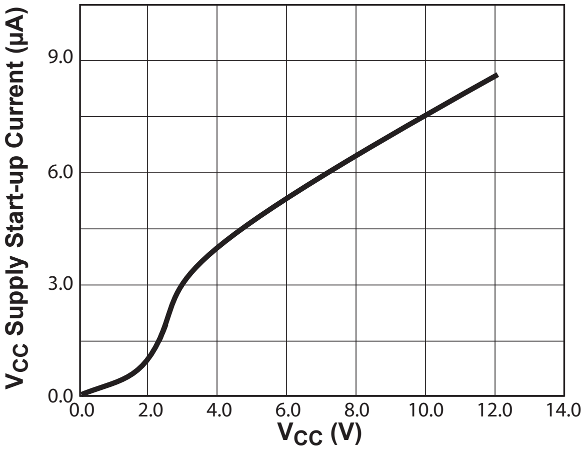


Figure 7.1 : V_{CC} vs. V_{CC} Supply Start-up Current

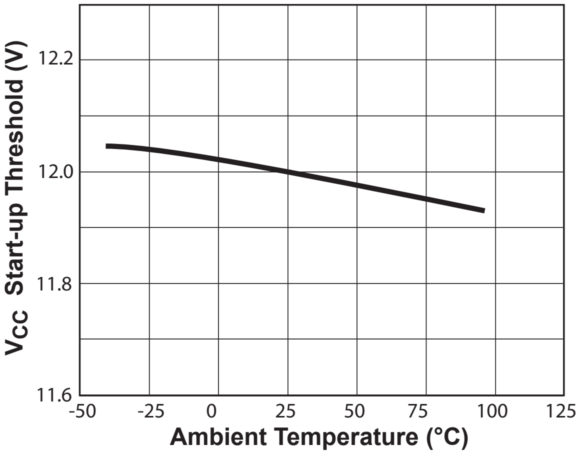


Figure 7.2 : Start-Up Threshold vs. Temperature

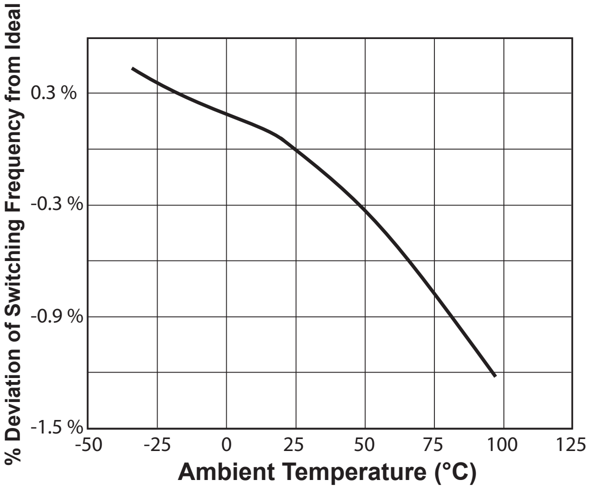


Figure 7.3 : % Deviation of Switching Frequency to Ideal Switching Frequency vs. Temperature

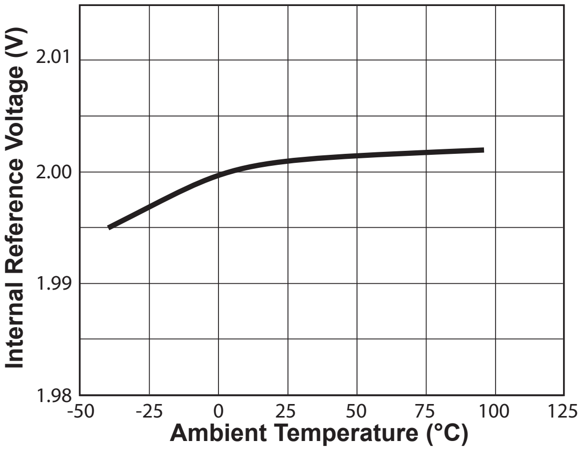


Figure 7.4 : Internal Reference vs. Temperature

8.0 Functional Block Diagram

iW3612 combines two functions: 1) wall dimmer type detection and dimmer phase measurement; and 2) output LED light dimming. It uses iWatt's proprietary digital control technology, which consists of: 1) chopping circuit, which helps to increase the power factor and serves as a dynamic impedance to load the dimmer; 2) primary side controlled isolated flyback converter. The iW3612 provides a low cost dimming solution which enables LED bulb to be used with most of the common wall dimmers. This allows LED bulbs to directly replace conventional incandescent bulbs with ease. The iW3612 can detect and operate with leading-edge, and trailing-edge dimmers as well as no-dimmer. The controller operates in critical discontinuous conduction mode (CDCM) to achieve high power efficiency and minimum EMI. It incorporates proprietary primary-feedback constant current control technology to achieve tight LED current regulation.

Figure 3.1 shows a typical iW3612 application schematic. Figure 8.1 shows the functional block diagram. The advanced digital control mechanism reduces system design time and improves reliability. The start-up algorithm makes sure the V_{CC} supply voltage is ready before powering up the IC.

The iW3612 provides multiple protection features for current limit, over-voltage protection, and over temperature protection. The V_T function can provide overtemperature compensation for the LED. The external NTC senses the LED temperature. If the V_T pin voltage is below $V_{P\text{-}LIM(HI)}$, the controller reduces the LED current. If the V_T pin voltage is below $V_{SH\text{-}TH}$ then the controller turns off.

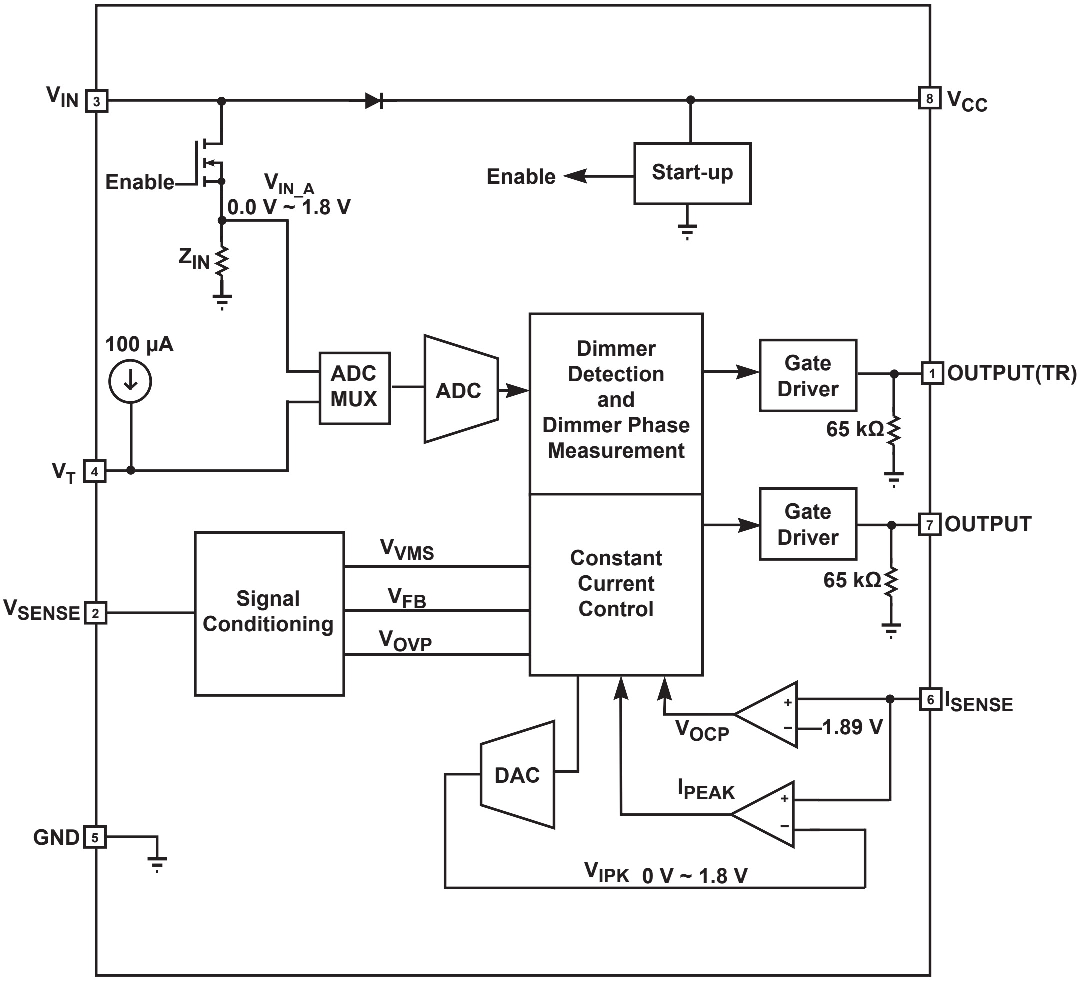


Figure 8.1 : iW3612 Functional Block Diagram

9.0 Theory of Operation

The iW3612 is a high performance AC/DC off-line power supply controller for dimmable LED luminaires, which uses advanced digital control technology to detect the dimmer type and dimmer phase to control the LED brightness. A PWM-dimming scheme is used to modulate the LED current with a dimming frequency of 900 Hz at low dimming levels. iW3612 can work with all types of wall dimmers including leading-edge dimmer, trailing-edge dimmer, as well as dimmer configurations such as R-type, R-C type or R-L type without visible flicker. The controller can also work when no dimmer is connected.

iW3612 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3612 includes a number of key built-in protection features. Using iWatt's state-of-the-art primary-feedback technology, the iW3612 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. iW3612 also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for accurate LED current regulation. Hence, the iW3612 can provide high performance dimming solutions, with minimal external component count and low bill of materials cost.

9.1 Pin Detail

Pin 1 – OUTPUT(TR)

Gate drive for the chopping circuit MOSFET switch.

Pin 2 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 3 – V_{IN}

Sense signal input from the rectified line voltage. V_{IN} is used for dimmer phase detection. The input line voltage is scaled down using a resistor network. It is used for input under-voltage and over-voltage protection. This pin also provides the supply current to the IC during start-up.

Pin 4 – V_T

External power limit and shutdown control. If the shutdown control is not used, this pin should be connected to GND via a resistor.

Pin 5 – GND

Ground.

Pin 6 – I_{SENSE}

Primary current sense. Used for cycle by cycle peak current control.

Pin 7 – OUTPUT

Gate drive for the external MOSFET switch.

Pin 8 – V_{CC}

Power supply for the controller during normal operation. The controller will start-up when V_{CC} reaches 12 V (typical) and will shut down when the V_{CC} voltage is below 7.5 V (typical). A decoupling capacitor should be connected between the V_{CC} pin and GND.

9.2 Wall Dimmer Detections

There are two types of wall dimmers: leading-edge dimmer and trailing-edge dimmer.

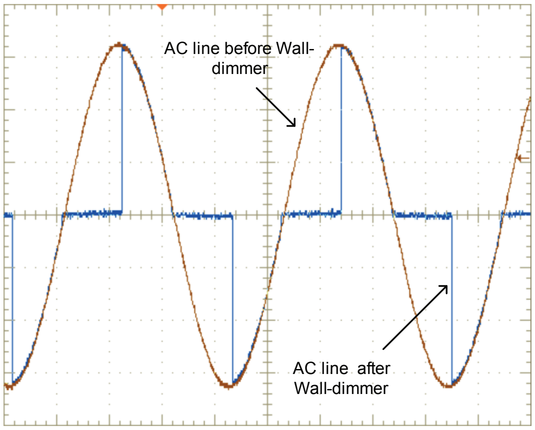


Figure 9.1 : Leading-Edge Wall Dimmer Waveforms

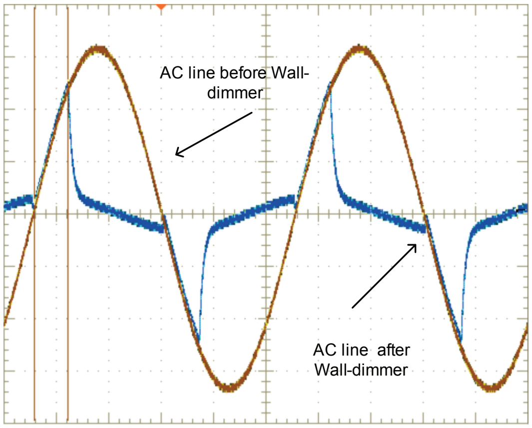


Figure 9.2 : Trailing-Edge Wall Dimmer Waveforms

Dimmer detection, or discovery, takes place during the third cycle after start-up. The controller determines whether no dimmer exists, or there is a leading edge dimmer or a trailing edge dimmer.

V_{CROSS} is internally generated by comparing the digitalized V_{IN} signal to the threshold of 0.14 V. The V_{IN} period (t_{PERIOD}) is measured between two consecutive rising edge zero-crossings. t_{CROSS} is generated by the internal digital block (refer to Figure 9.3); when V_{IN_A} is higher than 0.14 V t_{CROSS} is set to high and when V_{IN_A} falls below 0.14 V t_{CROSS} is reset to zero. If t_{CROSS} is much shorter than the V_{IN} period then a dimmer is detected. The controller uses the filtered derivatives to decide which type of dimmer is present. A large positive derivative value indicates a leading edge dimmer. Then the controller enters leading edge dimmer mode; otherwise it enters trailing edge dimmer mode.

During the dimmer detection stage, the OUTPUT(TR) keeps high to turn on the switch FET in the chopping circuit. This creates a resistive load for the wall dimmer.

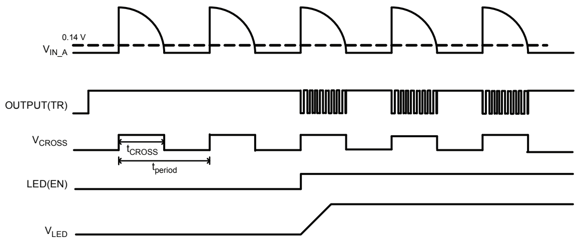


Figure 9.3 : Dimmer Detection

9.3 Dimmer Tracking and Phase Measurements

The dimmer detection algorithm and the dimmer tracking algorithm both depend on an accurate input voltage period measurement. The V_{IN} period is measured during the second cycle of the dimmer detection process and is latched for use thereafter. Using the measured V_{IN} period in subsequent calculations rather than a constant allows for automatic 50-/60-Hz operation and allows for a 10% frequency variation.

The phase measurement starts when V_{IN} exceeds the rising threshold until V_{IN} falls below the falling threshold.

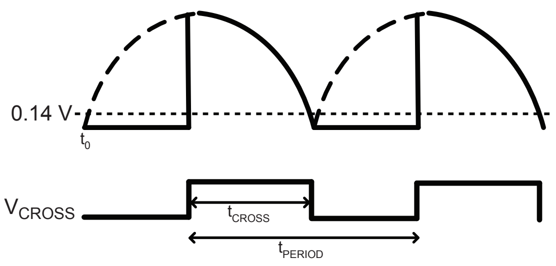


Figure 9.4 : Dimmer Phase Measurement

The dimmer phase is calculated as:

$$\text{Dimmer Phase} = \frac{t_{CROSS}}{t_{PERIOD}} \qquad (9.1)$$

The calculated dimmer phase is used to generate the signal D_{RATIO}, which determines LED current. If the dimmer phase is less than 0.14 then the D_{RATIO} is clamped at 0.14; if the dimmer phase is greater than 0.7 then D_{RATIO} is clamped at 1.0; otherwise D_{RATIO} is calculated by equation 9.2.

$$D_{RATIO} = \text{Dimmer Phase} \times K_1 - K_2 \qquad (9.2)$$

Where, K_1 is set to 1.768 and K_2 is set to 0.238.

Using $V_{Isense(NOM)}$ to represent the nominal 100% LED current, the V_{Isense}, which modulates the output LED current, is controlled by:

$$V_{Isense} = V_{Isense(NOM)} \times D_{RATIO} \qquad (9.3)$$

When D_{RATIO} is 1, the converter outputs 100% of nominal power to the LED. If D_{RATIO} is 0.01, the converter outputs 1% of nominal power to the LED.

9.4 Chopping Operation

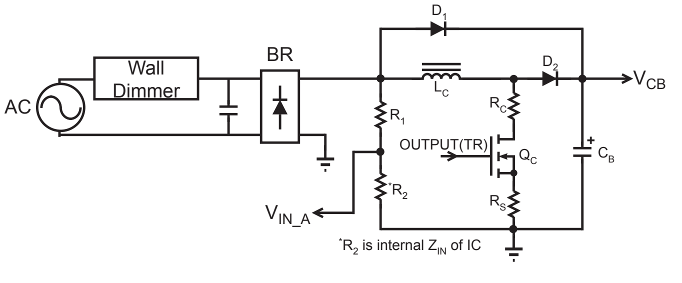


Figure 9.5 : Chopping Schematic

Chopping circuit provides the dynamic impedance for the dimmer and builds the energy to the LED power converter. It consists of L_C, Q_C, R_C, R_S, and D_2. L_C is the chopping inductor. During the chopping period, L_C is used to store the energy when the Q_C is on, and then release the energy to C_B when

Q_C is off. The on-time of Q_C during the chopping period when no dimmer exists is calculated by the following equation:

$$T_{ON(Qc)} = 4\mu s - 2.2\,{}^{\mu s}\!/_{V} \times V_{IN\_A} \tag{9.4}$$

The period of Q_C is calculated by:

$$T_{PERIOD(Qc)} = 12.2\mu s + 8.8\,{}^{\mu s}\!/_{V} \times V_{IN\_A} \tag{9.5}$$

V_{IN_A} is the scale voltage of V_{IN}. V_{CB} is the voltage across C_B. When t_{CROSS} is low, Q_C is always on. When t_{CROSS} is high, Q_C operates according to equation 9.4 and 9.5.

During the chopping period, the average current of L_C is in phase with the input AC line voltage, so it inherently generates high power factor. D_1 in the chopping circuit is used to charge C_B when the voltage of C_B is lower than the input line voltage. This helps to reduce the inrush current when the TRIAC is fired.

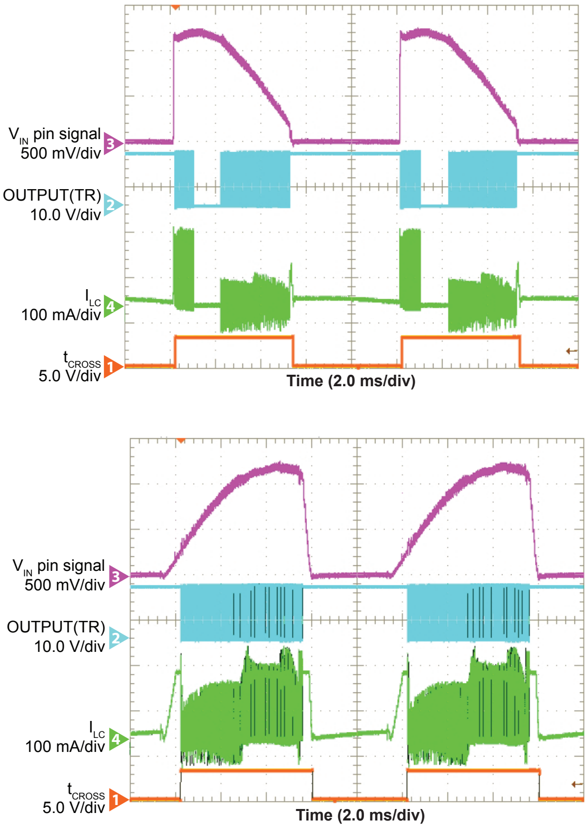


Figure 9.6 : Signals of Chopping Circuit

9.5 Start-up

Prior to start-up the V_{IN} pin charges up the V_{CC} capacitor through a diode between V_{IN} and V_{CC}. When V_{CC} is fully charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and enables the control logic, shown by Figure 9.7. When the control logic is enabled, the controller enters normal operation mode. During the first 3 half AC cycles, OUTPUT(TR) keeps high. After the dimmer type and AC line period are measured, the constant current stage is enabled and the output voltage starts to ramp up. When the output voltage is above the forward voltage of the LED, the controller begins to operate in constant current mode.

An adaptive soft-start control algorithm is applied during start-up state, where the initial output pulses are short and gradually get wider until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator.

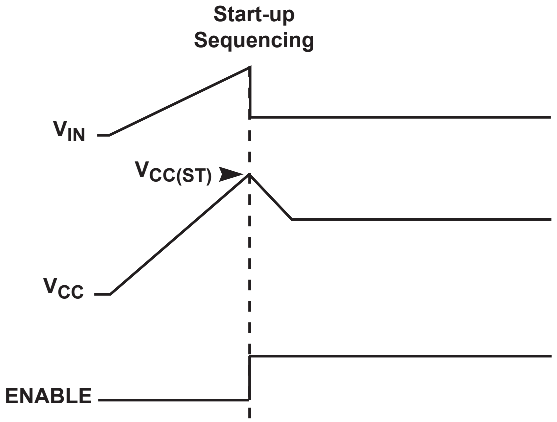


Figure 9.7 : Start-up Sequencing Diagram

9.6 Understanding Primary Feedback

Figure 9.8 illustrates a simplified flyback converter. When the switch Q_1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D_1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q_1 turns off, D_1 conducts and the stored energy $E_g(t)$ is delivered to the output.

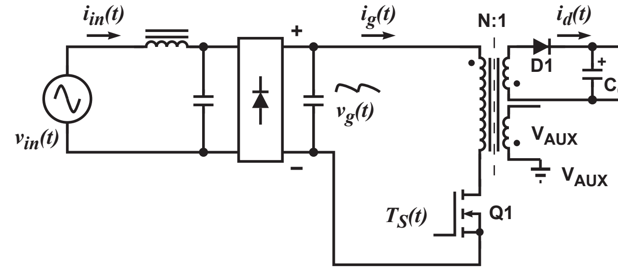


Figure 9.8 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \tag{9.6}$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \tag{9.7}$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \tag{9.8}$$

When Q_1 turns off, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \tag{9.9}$$

Assuming the secondary winding is master and the auxiliary winding is slave.

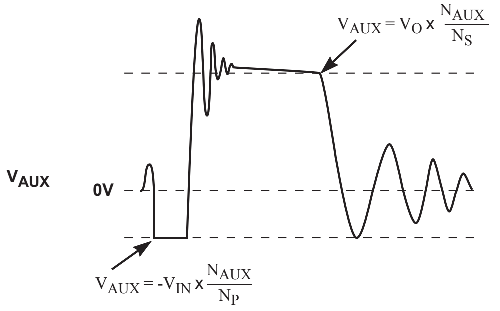


Figure 9.9 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \tag{9.10}$$

and reflects the output voltage as shown in Figure 9.9.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see Figure 9.9), then ΔV will also be small. With the iW3612, ΔV can be ignored.

The real-time waveform analyzer in the iW3612 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage and is used to regulate the output voltage.

9.7 Valley Mode Switching

In order to reduce switching losses in the MOSFET and EMI, the iW3612 employs valley mode switching during constant output current operation. In valley mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.10). By switching at the lowest V_{DS}, the switching loss will be minimized.

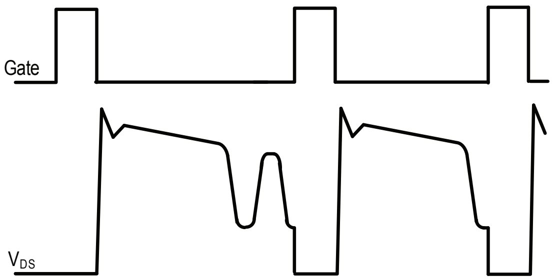


Figure 9.10 : Valley Mode Switching

Turning on at the lowest V_{DS} generates lowest dV/dt, thus valley mode switching can also reduce EMI. To limit the switching frequency range, the iW3612 can skip valleys (seen in the first cycle in Figure 9.10) when the switching frequency is greater than $f_{SW(MAX)}$.

At each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected.

9.8 LED Current Regulation

iW3612 incorporates a patented primary-side only constant current regulation technology. The iW3612 regulates the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode. To achieve this regulation the iW3612 senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground.

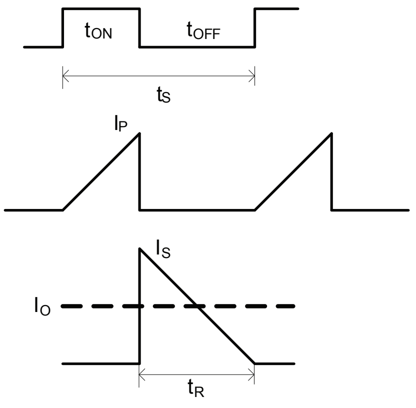


Figure 9.11 : Constant LED Current Regulation

The I_{SENSE} resistor determines the maximum current output of the power supply. The output current of the power supply is determined by:

$$I_{OUT} = \frac{1}{2} \times N_{PS} \times \frac{V_{REG-TH}}{R_{SENSE}} \times \frac{t_R}{t_S} \qquad (9.11)$$

where N_{PS} is the turns ratio of the primary and secondary windings and R_{SENSE} is the I_{SENSE} resistor.

9.9 V_{IN} Resistors

V_{IN} resistors are chosen primarily to scale down the input voltage for the IC. The scale factor for the input voltage in the IC is 0.0043 for high line, and 0.0086 for low line; if the internal impedance of this pin is selected to be 2.5 kΩ. Then for high line, the V_{IN} resistors should equate to:

$$R_{Vin} = \frac{2.5k\Omega}{0.0043} - 2.5k\Omega = 579k\Omega \qquad (9.12)$$

The V_{IN} resistors are shown in Figure 11.1 as R3 and R4.

9.10 Voltage Protection Functions

The iW3612 includes a function that protects against an input over-voltage (V_{IN} OVP) and output over-voltage (OVP).

The input voltage is monitored by V_{IN_A}, as shown in Figure 8.1. If this voltage exceeds 1.73 V for 15 continuous half AC cycles the iW3612 considers V_{IN} to be over-voltage. Output voltage is monitored by the V_{SENSE} pin. If the voltage at this pin exceeds $V_{SENSE(MAX)}$ for 2 continuous switching cycles the iW3612 considers the output voltage to be over-voltage

In both input over-voltage and output over-voltage cases, the IC shuts off immediately but remains biased to discharge the V_{CC} supply. In order to prevent overcharging the output voltage or overcharging the bulk voltage, the iW3612 employs an extended discharge time before restart. Initially if V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller attempts start-up three times.

Under the fault condition, the controller tries to start-up for three consecutive times. If all three start-up attempts fail, the controller enters the inactive mode, during which the controller does not respond to V_{CC} power-on requests. The controller will be activated again after it sees 29 start-up attempts. The controller can also be reset to the initial condition if V_{CC} is discharged. Typically, this extended discharge time is around 3 to 5 seconds.

This extended discharge time allows the iW3612 to support hot-plug LED modules without causing dangerously high output voltages while maintaining a quick recovery.

9.11 PCL, OC and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor short protection (SRSP) are features built-in to the iW3612. With the I_{SENSE} pin the iW3612 is able to monitor the primary peak current. This allows for cycle by cycle peak current control and limit. When the primary peak current multiplied by the I_{SENSE} sense resistor is greater than V_{OCP} over-current protection engages and the IC immediately turns off the gate drive until the next cycle. The output driver continues to send out switching pulses, but the IC will immediately turn off the gate drive if the OCP threshold is reached again.

If the I_{SENSE} sense resistor is shorted there is a potential danger of the over-current condition not being detected. Thus the IC is designed to detect this sense-resistor-short fault after the start up, and shutdown immediately. The V_{CC} will be discharged since the IC remains biased. In order to prevent overcharging the output voltage, the iW3612 employs an extended discharge time before restart, similar to the discharge time described in section 9.10.

9.12 Over Temperature Protection

If an NTC thermistor is connected from the V_T pin to GND then, the iW3612 is able to detect and protect against an over temperature event (OTP).

The iW3612 provides a current (I_{VT}) to the V_T pin and detects the voltage on the pin. Based on this voltage the iW3612 can monitor the temperature on the NTC thermistor. As the V_T pin voltage reduces, the iW3612 reduces the amount of chopping and the output current according to Figure 9.12.

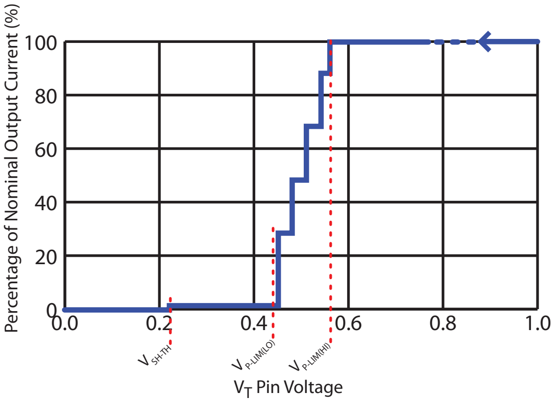


Figure 9.12 : V_T Pin Voltage vs. % of Nominal Output Current V_T from 1.0 V to 0.0 V

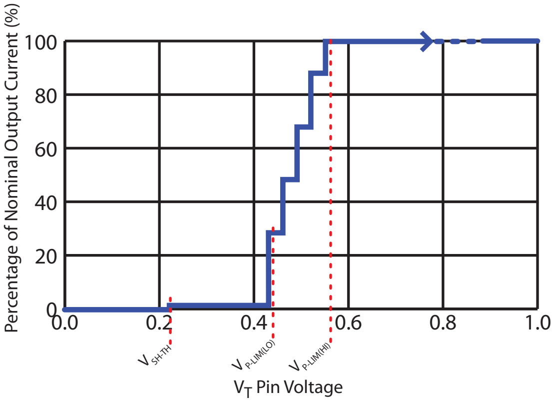


Figure 9.13 : V_T Pin Voltage vs. % of Nominal Output Current V_T from 0.0 V to 1.0 V

When the V_T pin voltage reaches $V_{P\text{-}LIM(HI)}$ the output current begins to reduce as shown in Figure 9.12. At $V_{P\text{-}LIM(LO)}$ the output current reduces to 1%. The device can be placed in shutdown mode by pulling the V_T pin to ground or below $V_{SH\text{-}TH}$.

9.13 Thermal Design

The iW3612 is typically installed inside a small enclosure, where space and air volumes are constrained. Under these circumstances θ_{JA} (thermal resistance, junction to ambient) measurements do not provide useful information for this type of application. Instead we have provided ψ_{JB} which estimates the increase in die junction temperature relative to the PCB surface temperature. Figure 9.14 shows the PCB surface temperature is measured at the IC's GND pin pad.

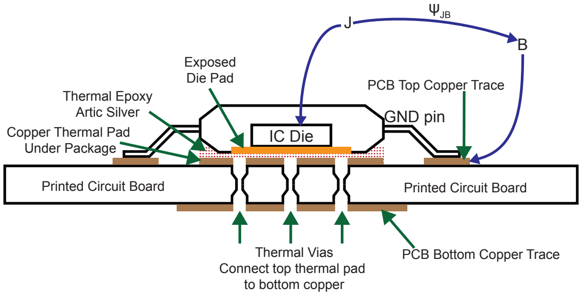


Figure 9.14 : Ways to Improve Thermal Resistance

Using ψ_{JB} the junction temperature (T_J) of the IC can be found using the equation below.

$$T_J = T_B + P_H \cdot \Psi_{JB} \tag{9.13}$$

where, T_B is the PCB surface temperature and P_H is the power applied to the chip or the product of V_{CC} and I_{CCQ}.

The iW3612 uses an exposed pad package to reduce the thermal resistance of the package. The exposed pad can be electrically connected to the GND pin of the IC. Although by having an exposed package can provide some thermal resistance improvement, more significant improvements can be obtained with simple PCB layout and design. Figure 9.14 demonstrates some recommended techniques to improve thermal resistance, which are also highlighted below.

Ways to Improve Thermal Resistance

- Increase PCB area and associated amount of copper interconnect.
- Use thermal adhesive to attach the package to a thermal pad on PCB.
- Connect PCB thermal pad to additional copper on PCB using thermal vias.

Environment	ψ_{JB}
No adhesive	70 °C/W
Use thermal adhesive to pad	63 °C/W
Use thermal adhesive to pad with thermal vias	49 °C/W

Table 9.1 : Improvements in ψ_{JB} Based on Limited Experimentation

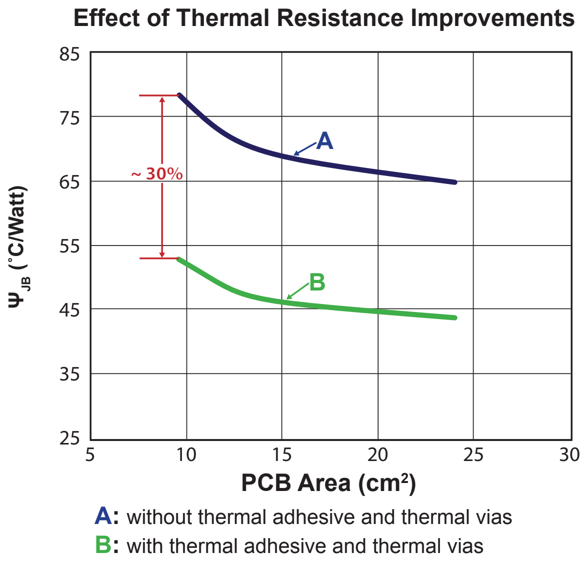
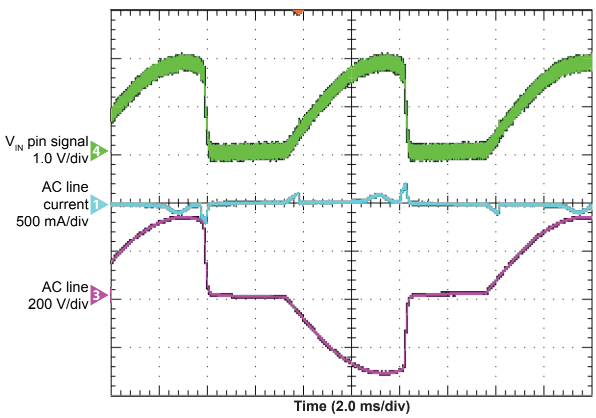


Figure 9.15 : Effect of Thermal Resistance Improvements

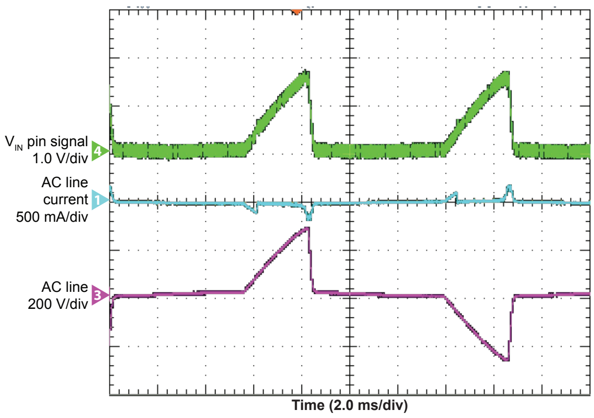
Figure 9.15 shows improvement of approximately 30% in thermal resistance across different PCB sizes when the exposed pad is attached to PCB using a thermal adhesive and thermal vias connect the pad to a larger plate on the opposing side of the PCB.

10.0 Performance Characteristics



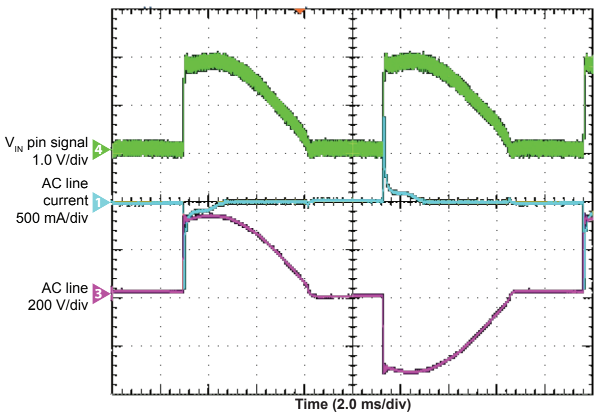
Trailing Edge Dimmer

Figure 10.1 : Trailing Edge Dimmer



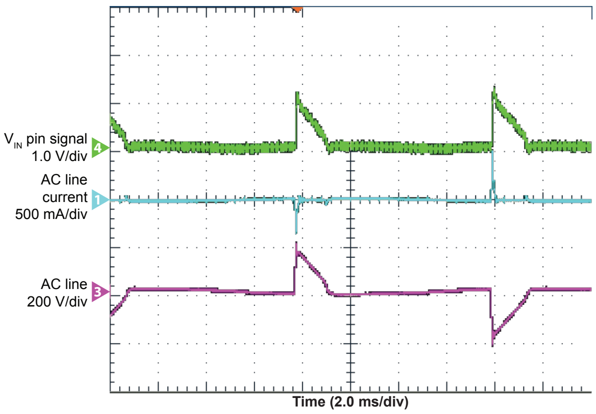
Trailing Edge Dimmer

Figure 10.2 : Trailing Edge Dimmer 2



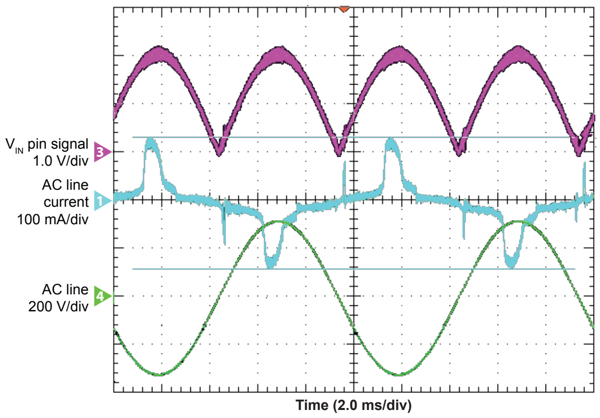
Leading Edge Dimmer

Figure 10.3 : Leading Edge Dimmer



Leading Edge Dimmer

Figure 10.4 : Leading Edge Dimmer 2



No Dimmer

Figure 10.5 : No Dimmer

11.0 Typical Application Schematic

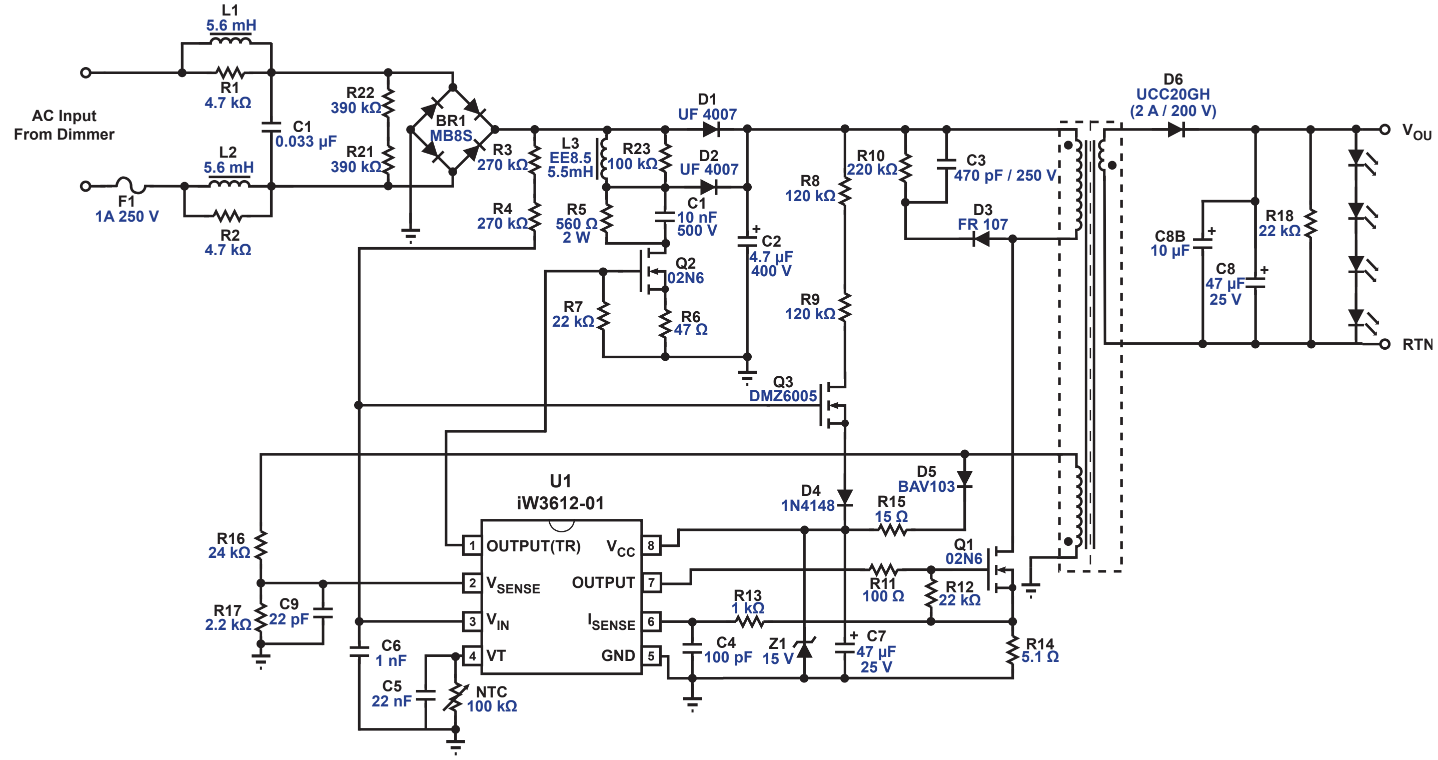
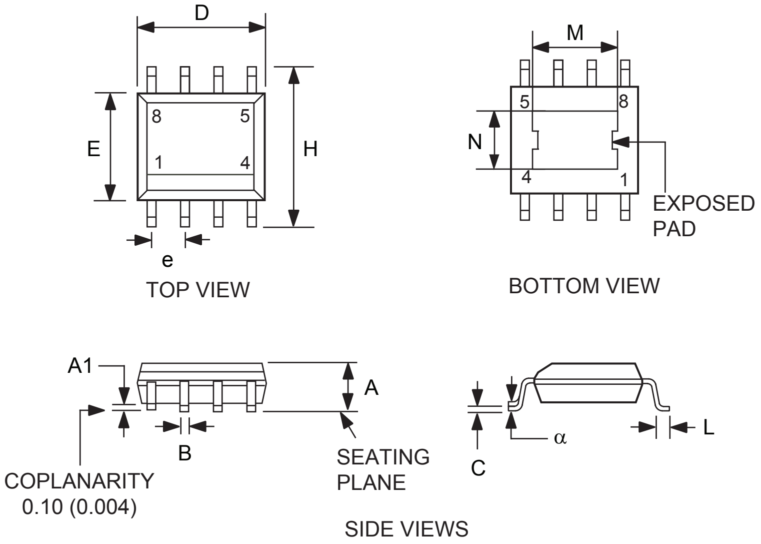


Figure 11.1 : Schematic of a 13-V, 350-mA Dimmable LED Driver for 230-V_{AC} Application

12.0 Physical Dimensions

8-Lead Small Outline (SOIC) Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.051	0.067	1.30	1.70
A1	0.0020	0.0060	0.05	0.150
B	0.014	0.019	0.36	0.48
C	0.007	0.010	0.18	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.79	6.20
N	0.086	0.094	2.18	2.39
M	0.118	0.126	3.00	3.20
L	0.016	0.050	0.41	1.27
α	0°	8°		

Figure 12.1 : Physical dimensions, 8-lead SOIC package

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E are determined at the outermost extremes of the plastic bocy exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

13.0 Ordering Information

Part Number	Options	Package	Description
iW3612-00	Optimized for 100 V_{AC} Applications[2]	SOIC-8 (exposed pad)	Tape & Reel[1]
iW3612-01	Optimized for 230 V_{AC} Applications[2]	SOIC-8 (exposed pad)	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel.

Note 2: Refer to Section 9.4 Chopping Operation for more information.

About iWatt

iWatt Inc. is a fabless semiconductor company that develops intelligent power management ICs for computer, communication, and consumer markets. The company's patented *pulseTrain*™ technology, the industry's first truly digital approach to power system regulation, is revolutionizing power supply design.

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