

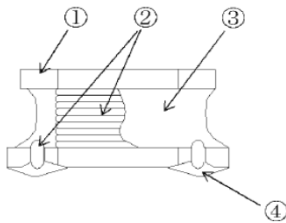
SERIES LIST

No.	Part No.	L (μH)	Tol.	RDC (Ω) $\pm 20\%$	Isat (A)	Irms (A)
1	JNR 4018H-R47N	0.47	$\pm 30\%$	0.015	6.00	5.50
2	JNR 4018H-R56N	0.56	$\pm 30\%$	0.019	5.00	4.50
3	JNR 4018H-1R0N	1.0	$\pm 30\%$	0.027	4.00	3.20
4	JNR 4018H-1R2N	1.2	$\pm 30\%$	0.030	3.70	2.80
5	JNR 4018H-1R5N	1.5	$\pm 30\%$	0.037	3.30	2.40
6	JNR 4018H-1R8M	1.8	$\pm 20\%$	0.040	3.20	2.30
7	JNR 4018H-2R2M	2.2	$\pm 20\%$	0.042	3.00	2.20
8	JNR 4018H-2R7M	2.7	$\pm 20\%$	0.050	2.60	2.10
9	JNR 4018H-3R3M	3.3	$\pm 20\%$	0.055	2.30	2.00
10	JNR 4018H-4R7M	4.7	$\pm 20\%$	0.070	2.00	1.70
11	JNR 4018H-6R8M	6.8	$\pm 20\%$	0.098	1.60	1.45
12	JNR 4018H-7R5M	7.5	$\pm 20\%$	0.120	1.50	1.35
13	JNR 4018H-100M	10	$\pm 20\%$	0.150	1.30	1.20
14	JNR 4018H-150M	15	$\pm 20\%$	0.210	1.10	0.85
15	JNR 4018H-220M	22	$\pm 20\%$	0.290	0.90	0.72
16	JNR 4018H-330M	33	$\pm 20\%$	0.460	0.70	0.55
17	JNR 4018H-470M	47	$\pm 20\%$	0.650	0.60	0.44
18	JNR 4018H-680M	68	$\pm 20\%$	1.000	0.52	0.32

Note:

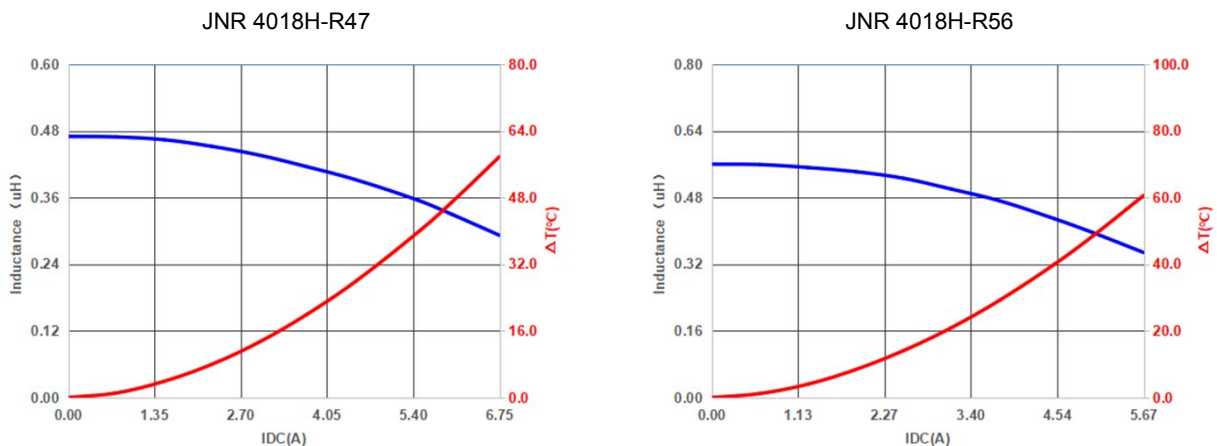
1. Test Frequency : 100KHz /1V
2. All test data referenced to 25°C ambient
3. Isat : Saturation Current (Isat) will cause L0 to drop approximately 30%.
4. Irms : Heat Rated Current (Irms) will cause the coil temperature rise approximately ΔT of 40°C
5. Rated DC current : The lower value of Irms and Isat.

Materials

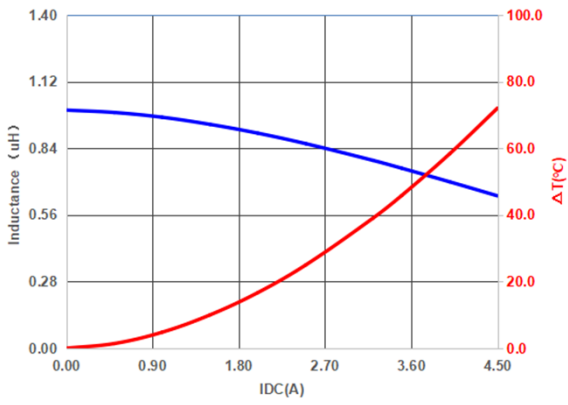


No.	Description	Specification
1	Core	Ferrite Core
2	Wire	Enameled Copper Wire
3	Glue	Epoxy with magnetic powder
4	Terminal	Ag/Ni/Sn+Sn Solder

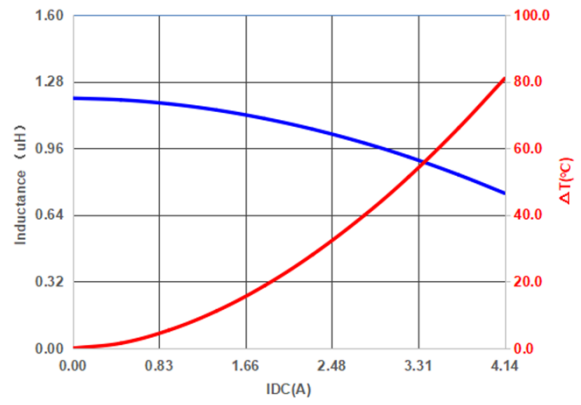
TYPICAL PERFORMANCE CURVES



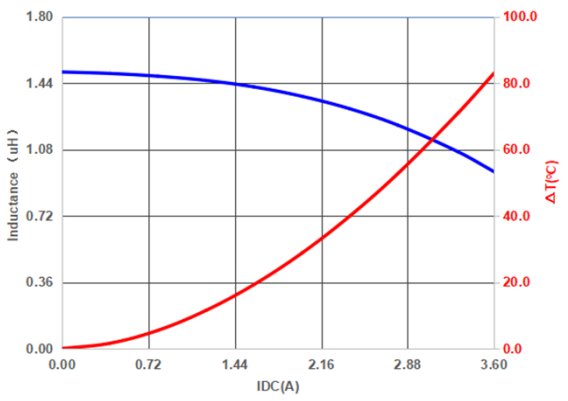
JNR 4018H-1R0



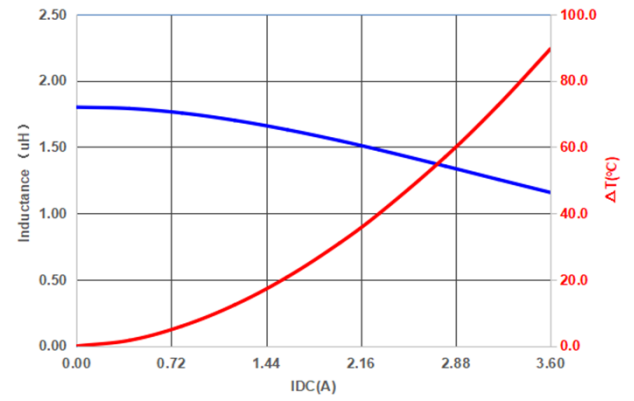
JNR 4018H-1R2



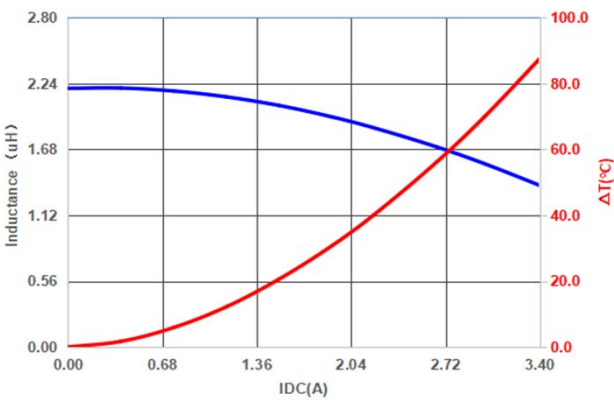
JNR 4018H-1R5



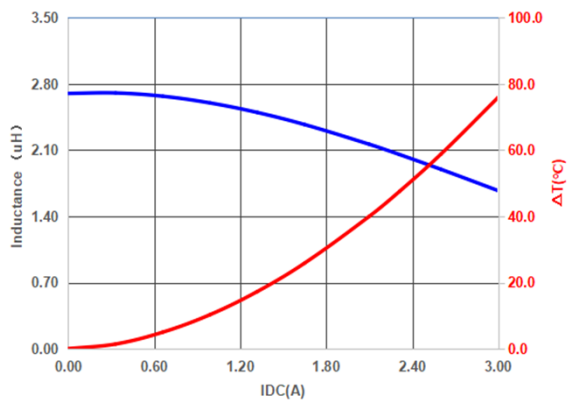
JNR 4018H-1R8



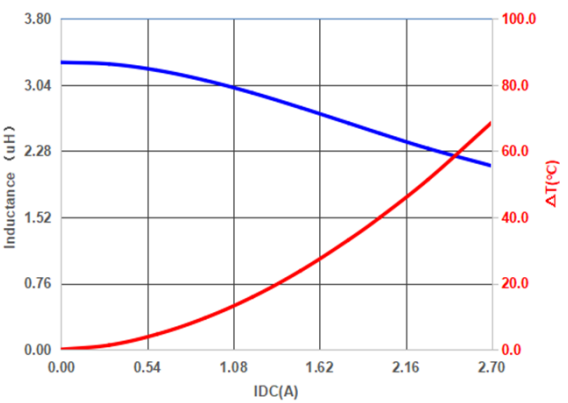
JNR 4018H-2R2



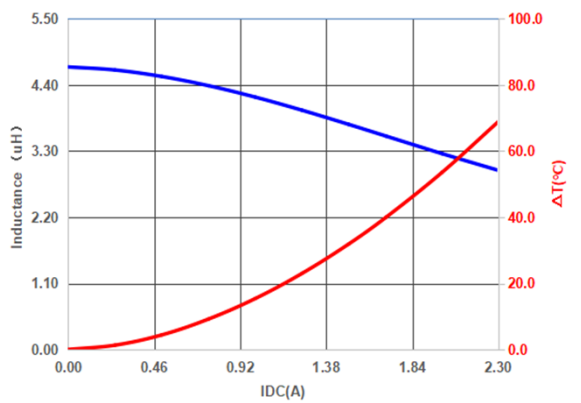
JNR 4018H-2R7



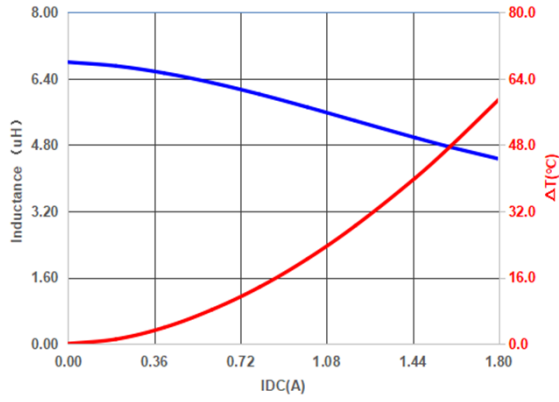
JNR 4018H-3R3



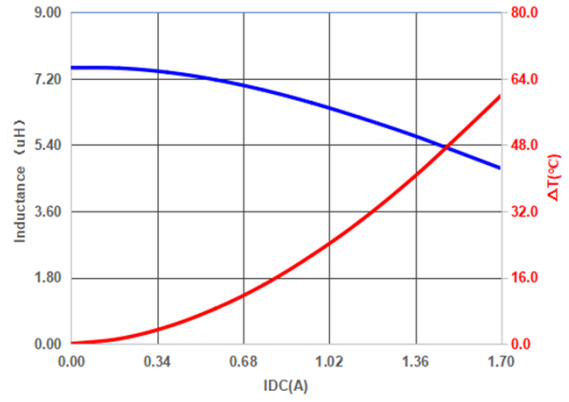
JNR 4018H-4R7



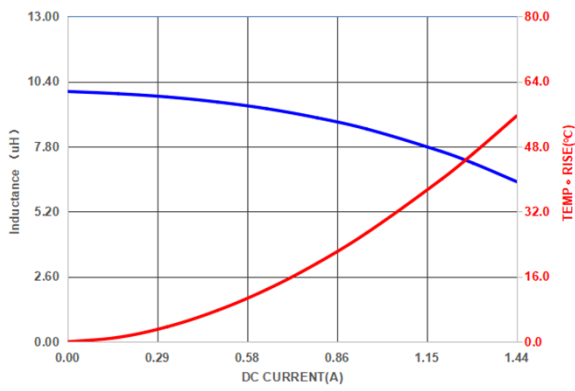
JNR 4018H-6R8



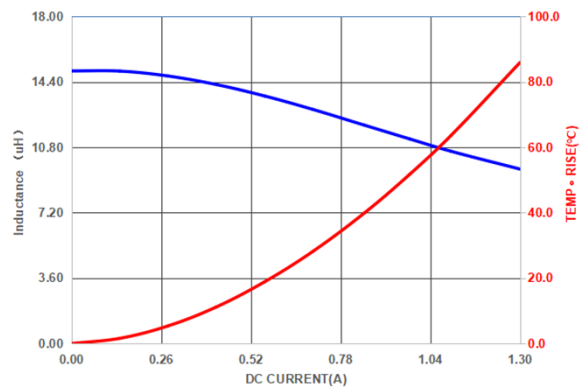
JNR 4018H-7R5



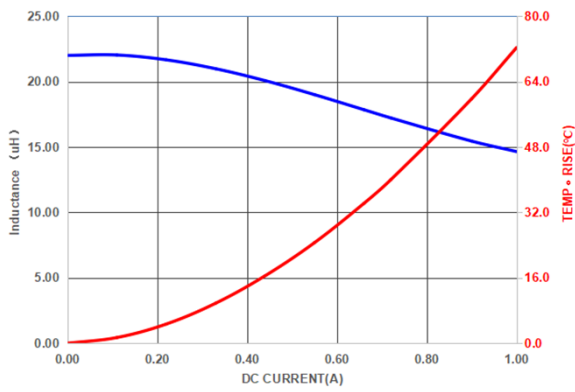
JNR 4018H-100



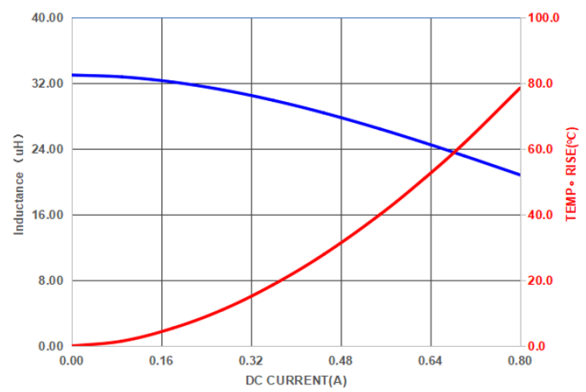
JNR 4018H-150



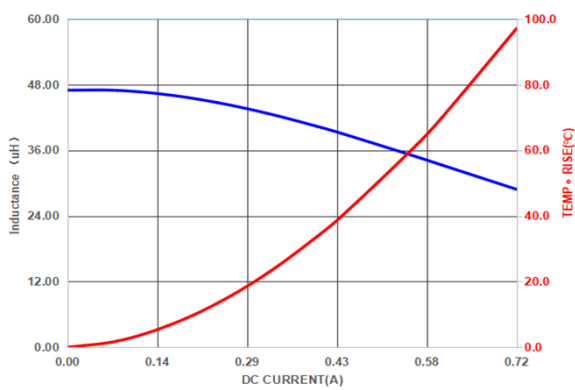
JNR 4018H-220



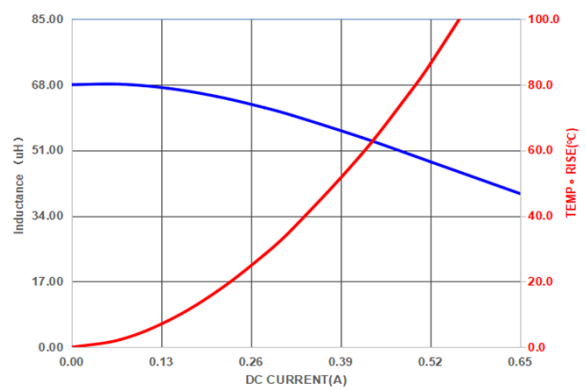
JNR 4018H-330



JNR 4018H-470



JNR 4018H-680



■ Appearance criterion

1 - Core chipping

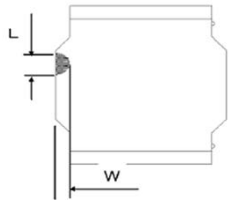
The appearance standard of the chipping size on top side, and bottom side ferrite core is listed below.

Chip off is generated during molding and manufacturing process.

Chip off acceptance limits subjected to the product size.

Our current Defect limit is based on the IPC-A-610.

Some chip off does not impact the product function, see the IPC standard 1 & 2.

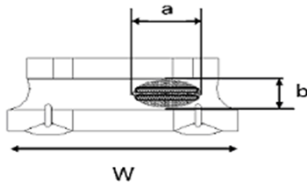


L	≤50 % of the length
W	≤25 % of the width

Defects usually occur at the corners and edges of the product, There will be a slight defect black and rough, but not exposed copper, and does not affect the product performance and reliability.

2 - Void appearance tolerance Limit

Size of voids occurring to coating resin is specified below.



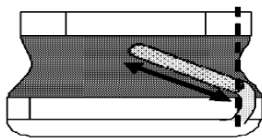
Exposed wire tolerance limit of coating resin part on product side.

Size of exposed wire occurring to coating resin is specified below.

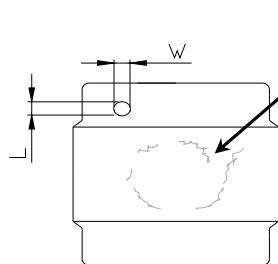
1. Width direction (dimension a) : Acceptable when $a \leq w/2$.
2. Length direction (dimension b) : Dimension b is not specified.
3. The total area of exposed wire occurring to each sides is not greater than 50% of coating resin area, and is acceptable.

3 - External appearance criterion for exposed wire


Exposed winding wire at the secondary side is regarded as qualified product.




4、 Electrode appearance criterion for exposed wire



Visual check on core surface with no crack means pass.


 Only top side of wire is exposed.
 (regardless of whole top side of wire exposed)

Conforming


 Wire is soldered insufficiently and less than half of outer diameter is covered with solder.

Less than 1/2 of joint side length.
(More than 1/2 is selected as defect)

L & W
≤ 20% of the area on one single pad

Foreign materials on the product body is inevitable and accepted.

Electrodes with foreign body (dirt) appearance standards

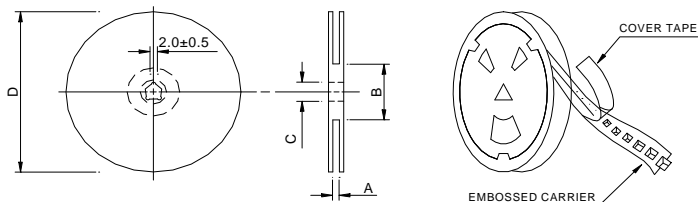
Foreign materials (dirt) will not affect the coplanarity of PAD,

below the example of foreign materials (dirt) quantity ≤2PCS on single PAD.

Dimensions range as shown in the table.

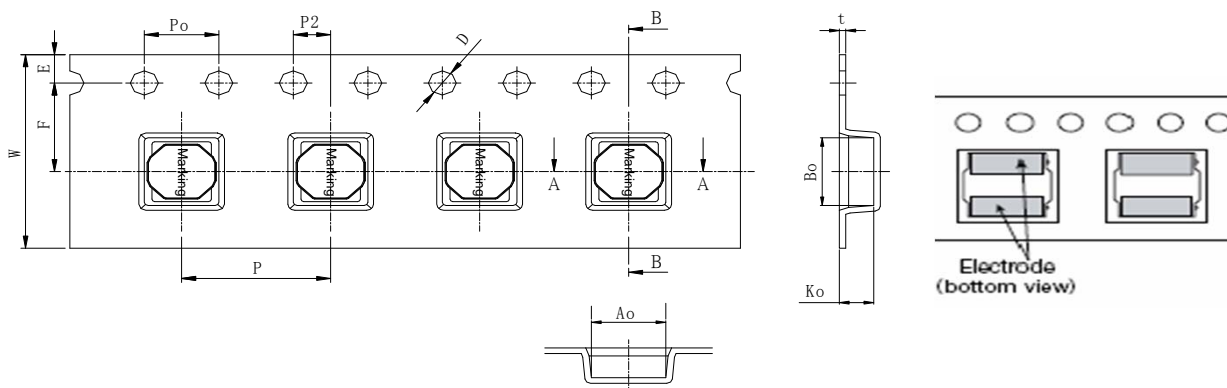
Packaging Information

• Reel Dimension



Type	A(mm)	B(mm)	C(mm)	D(mm)
13"x12mm	13.4+2-0	80±2.0	13+0.5/-0.2	330±3.0

• Tape Dimension



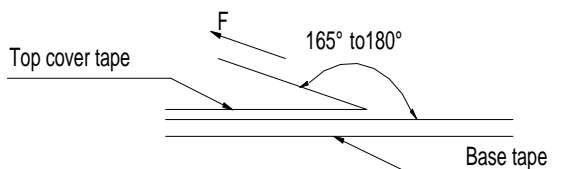
Ao(mm)	Bo(mm)	Ko(mm)	P(mm)	Po(mm)	P2(mm)	w(mm)	t(mm)	Emm	F(mm)	D(mm)
4.4±0.1	4.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	2.00±0.1	12±0.3	0.35±0.1	1.75±0.1	5.50±0.1	1.5±0.1

• Packaging Quantity

Size	Reel
JNR 4018H	3500

• Tearing Off Force

The force for tearing off cover tape is 10 to 130 grams in the arrow direction under the following conditions (referenced ANSI/EIA-481-D-2008 of 4.11 standard).



Tearing Speed mm	Room Temp. (°C)	Room Humidity (%)	Room atm (hPa)
300±10%	5~35	45~85	860~1060

Application Notice

- Storage Conditions(component level)

To maintain the solderability of terminal electrodes:

1. Products meet IPC/JEDEC J-STD-020E standard-MSL, level 1.
2. Temperature and humidity conditions: Less than 40°C and 60% RH.
3. Recommended products should be used within 12 months form the time of delivery.
4. The packaging material should be kept where no chlorine or sulfur exists in the air.

- Transportation

1. Products should be handled with care to avoid damage or contamination from perspiration and skin oils.
2. The use of tweezers or vacuum pick up is strongly recommended for individual components.
3. Bulk handling should ensure that abrasion and mechanical shock are minimized.

Reliability and Test Condition

Item	Performance	Test Condition
Electrical Performance Test		
Inductance	Refer to standard electrical characteristics list	HP4284A,CH11025,CH3302,CH1320,CH1320S LCR Meter
DCR		CH16502,Agilent33420A Micro-Ohm Meter
Saturation Current (Isat)	Approximately $\Delta L30\%$.	Saturation DC Current (Isat) will cause L0 to drop $\Delta L(\%)$
Heat Rated Current (Irms)	Approximately $\Delta T40^{\circ}\text{C}$	Heat Rated Current (Irms) will cause the coil temperature rise $\Delta T(^{\circ}\text{C})$ without core loss. 1.Applied the allowed DC current 2.Temperature measured by digital surface thermometer
Operating Temperature	-40 $^{\circ}\text{C}$ ~+125 $^{\circ}\text{C}$ (Including self - temperature rise)	
Storage Temperature	1.-10~+40 $^{\circ}\text{C}$,50~60%RH (Product without taping) 2.-40~+125 $^{\circ}\text{C}$ (on board)	
Reliability Test		
Life Test	Appearance : No damage Inductance : within $\pm 10\%$ of initial value Q : Shall not exceed the specification value RDC : within $\pm 15\%$ of initial value and shall not exceed the specification value	Preconditioning: Run through IR reflow for 2 times. (IPC/JEDEC J-STD-020D Classification Reflow Profiles) Temperature : 125 $\pm 2^{\circ}\text{C}$ (Inductor) Applied current : rated current Duration : 1000 ± 12 hrs Measured at room temperature after placing for 24 ± 2 hrs
Load Humidity		Preconditioning: Run through IR reflow for 2 times. (IPC/JEDEC J-STD-020D Classification Reflow Profiles) Humidity : 85 $\pm 2\%$ R.H Temperature : 85 $^{\circ}\text{C} \pm 2^{\circ}\text{C}$ Duration : 1000hrs Min. with 100% rated current Measured at room temperature after placing for 24 ± 2 hrs
Moisture Resistance		Preconditioning: Run through IR reflow for 2 times. (IPC/JEDEC J-STD-020D Classification Reflow Profiles) 1. Baked at50 $^{\circ}\text{C}$ for 25hrs, measured at room temperature after placing for 4 hrs. 2. Raise temperature to 65 $\pm 2^{\circ}\text{C}$ 90-100%RH in 2.5hrs, and keep 3 hours, cool down to 25 $^{\circ}\text{C}$ in 2.5hrs. 3. Raise temperature to 65 $\pm 2^{\circ}\text{C}$ 90-100%RH in 2.5hrs, and keep 3 hours, cool down to 25 $^{\circ}\text{C}$ in 2.5hrs, keep at 25 $^{\circ}\text{C}$ for 2 hrs then keep at -10 $^{\circ}\text{C}$ for 3 hrs 4. Keep at 25 $^{\circ}\text{C}$ 80-100%RH for 15min and vibrate at the frequency of 10 to 55 Hz to 10 Hz, measure at room temperature after placing for 1~2 hrs.
Thermal shock		Preconditioning: Run through IR reflow for 2 times. (IPC/JEDEC J-STD-020D Classification Reflow Profiles) Condition for 1 cycle Step1 : -40 $\pm 2^{\circ}\text{C}$ 30 ± 5 min Step2 : 25 $\pm 2^{\circ}\text{C}$ ≤ 0.5 min Step3 : 125 $\pm 2^{\circ}\text{C}$ 30 ± 5 min Number of cycles : 500 Measured at room temperature after placing for 24 ± 2 hrs
Vibration		Oscillation Frequency: 10~2K~10Hz for 20 minutes Equipment : Vibration checker Total Amplitude:1.52mm $\pm 10\%$ Testing Time : 12 hours(20 minutes, 12 cycles each of 3 orientations) °

Reliability and Test Condition

Item	Performance	Test Condition																		
Reliability Test																				
Shock	Appearance : No damage. Inductance : within±10% of initial value Q : Shall not exceed the specification value RDC : within ±15% of initial value and shall not exceed the specification value	<table border="1"> <thead> <tr> <th rowspan="2">Type</th> <th>Peak value</th> <th>Normal</th> <th rowspan="2">Wave form</th> <th>Velocity</th> </tr> <tr> <th>(g's)</th> <th>duration (D) (ms)</th> <th>change (V)ft/sec</th> </tr> </thead> <tbody> <tr> <td>SMD</td> <td>50</td> <td>11</td> <td>Half-sine</td> <td>11.3</td> </tr> <tr> <td>Lead</td> <td>50</td> <td>11</td> <td>Half-sine</td> <td>11.3</td> </tr> </tbody> </table>	Type	Peak value	Normal	Wave form	Velocity	(g's)	duration (D) (ms)	change (V)ft/sec	SMD	50	11	Half-sine	11.3	Lead	50	11	Half-sine	11.3
Type		Peak value		Normal	Wave form		Velocity													
	(g's)	duration (D) (ms)	change (V)ft/sec																	
SMD	50	11	Half-sine	11.3																
Lead	50	11	Half-sine	11.3																
Bending		Shall be mounted on a FR4 substrate of the following dimensions: >=0805:40x100x1.2mm <0805:40x100x0.8mm Bending depth: >=0805:1.2mm <0805:0.8mm duration of 10 sec.																		
Soderability	More than 95% of the terminal electrode should be covered with solder	Preheat: 150°C,60sec Solder: Sn96.5% Ag3% Cu0.5% Temperature: 245±5°C Flux for lead free: Rosin. 9.5% Dip time: 4±1sec Depth: completely cover the termination																		
Resistance to Soldering Heat		Number of heat cycles: 1 <table border="1"> <thead> <tr> <th>Temperature (°C)</th> <th>Time (s)</th> <th>Temperature ramp/immersion and emersion rate</th> </tr> </thead> <tbody> <tr> <td>260 ±5 (solder temp)</td> <td>10 ±1</td> <td>25mm/s ±6 mm/s</td> </tr> </tbody> </table>	Temperature (°C)	Time (s)	Temperature ramp/immersion and emersion rate	260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s												
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260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s																		
Terminal Strength	Appearance : No damage. Inductance : within±10% of initial value Q : Shall not exceed the specification value RDC : within ±15% of initial value and shall not exceed the specification value	Preconditioning:Run through IR reflow for 2 times (IPC/JEDEC J-STD-020D Classification Reflow Profiles) With the component mounted on a PCB with the device to be tested, apply a force (>0805:1kg , <=0805:0.5kg)to the side of a device being tested. This force shall be applied gradually for 60 +1 seconds. Also the force shall be applied gradually as not to apply a shock to the component being tested. 																		

Note : When there are questions concerning measurement result measurement shall be made after 48 ± 2 hours Of recovery under the standard condition.

Reliability and Test Condition

Item	Performance	Test Condition
Reliability Test		
Soldering	Mildly activated rosin fluxes are preferred. JANTEK terminations are suitable for all wave and re-flow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.	
Lead Free Solder re-flow:	Recommended temperature profiles for re-flow soldering in Figure 1.	
Soldering Iron(Figure 2):	<p>Products attachment with a soldering iron is discouraged due to the inherent process control limitations.</p> <p>In the event that a soldering iron must be employed the following precautions are recommended.</p> <p>Note :</p> <ul style="list-style-type: none"> • Preheat circuit and products to 150°C • Never contact the ceramic with the iron tip • Use a 20 watt soldering iron with tip diameter of 1.0mm • 355°C tip temperature (max) • 1.0mm tip diameter (max) • Limit soldering time to 4~5 sec 	

Reflow Soldering

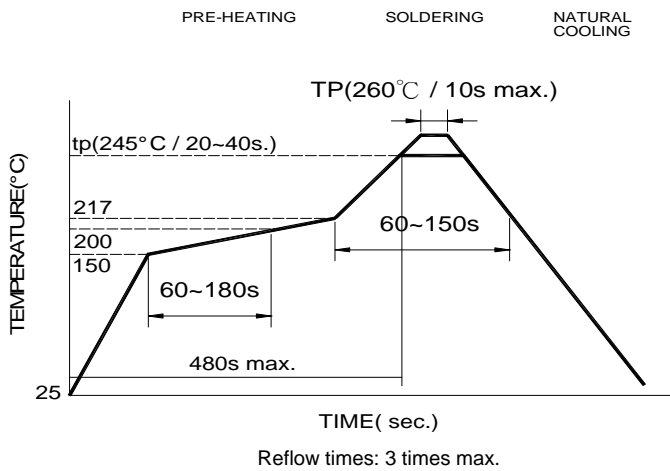


Fig.1

Iron Soldering

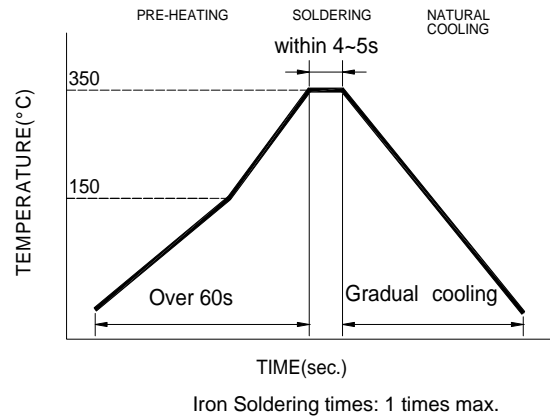


Fig.2