CMT804x High-Speed, Reinforced Quad-Channel Digital Isolator

1 Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL 1577 component recognition program
  - CSA certification according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 end equipment standards
  - CQC approval per GB4943.1-2011
  - TUV certification according to EN 60950-1, EN 62368-1 and EN 61010-1
- Robust electromagnetic compatibility
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Data rate: up to 150 Mbps
- Wide supply range: 2.5 to 5.5 V
- Operation temperature: -40°C to 125°C
- Robust isolation barrier
  - More than 40-year projected lifetime
  - Up to 5 kV_{RMS} isolation rating
  - Up to 8 kV surge capability
  - ±150 kV/μs typical CMTI
- Default output high or low options
- Low power consumption, typical 2.5 mA per channel at 1 Mbps
- Low propagation delay: 9 ns typical (5V supplies)
- SOIC 16 package (wide body and narrow body)

2 Applications

- Industrial automatic control
- New energy vehicles
- Solar inverters
- Motor control
- Isolated SPI
- General purpose multichannel isolation

3 Description

The CMT804x series devices are high-performance, quad channel digital isolators with as high as 5 kV_{rms} isolation voltage by means of silicon-dioxide (SiO2) insulation barrier.

The digital isolator is used to communicate between two different power supply domains while prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

This device comes with enable pins that can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The CMT804x device has four forward and up to two reverse-direction channels. If the input power or signal is lost, the default output is high for the CMT804x1 device and low for the CMT804x0 device. See the Device Functional Modes section for further details.

The isolator provides high electromagnetic immunity and low emissions at low-power consumption. Through innovative chip design and layout techniques, electromagnetic compatibility of the CMT804x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

The CMT804x series device is available in both narrow-body (NB) and wide-body (WB) 16-pin SOIC packages.

Device Information

Part No.	Package	Body Size (mm x mm)
CMT804x	NB(N) SOIC-16	9.9 x 3.9
	WB(W) SOIC-16	10.4 x 7.5
Refer to section 14 for ordering information.		

Simplified Schematic

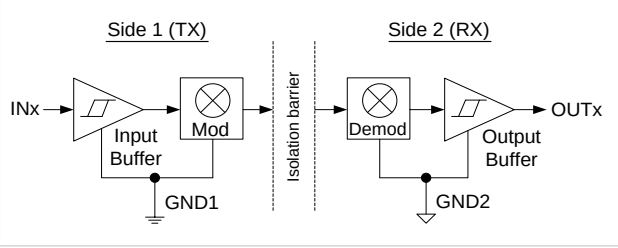


Table of Contents

4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage[2]	VDD1, VDD2		-0.5	6.5	V
Maximum input voltage	INx, EN1, EN2	x = A, B, C, D	-0.4	VDD+0.4	V
Maximum output voltage	OUTx	x = A, B, C, D	-0.4	VDD+0.4	V
Maximum Input / output pulse voltage	-	Pulse width should be less than 100 ns, and the duty cycle should be less than 10%	-0.8	VDD+0.8	V
Common-mode transients immunity	CMTI			±150	kV/us
Output current	I_O		-15	15	mA
Maximum surge immunity	-			8	kV
Operating temperature	T_A		-40	125	℃
Storage temperature	T_{STG}		-40	150	℃

Notes:

[1]. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

[2]. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

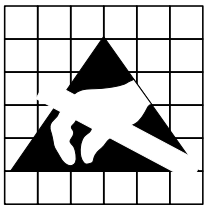
Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD1, VDD2		2.5	5	5.5	V
High level input voltage	V_{IH}	VDDI: input side VDD	2		VDDI	V
Low level input voltage	V_{IL}	VDDI: input side VDD	0		0.8	V
Data rate	DR		0		150	Mbps
Operating temperature	T_A		-40	25	125	℃
Junction temperature	T_J		-40		150	℃

6 ESD Ratings

Table 3. ESD Ratings

Parameter	Symbol	Condition	Max.	Unit
Electrostatic discharge	V_{ESD}	Human-body model (HBM)	±8000	V
		Charged-device model (CDM)	± 2000	

Notes:
1. IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
2. Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

7 Pin Description

Both narrow-body (N) and wide-body (W) 16-pin SOIC packages are available for the series part number CMT8040x, CMT8041x and CMT8042x. The pin lists are shown as below.

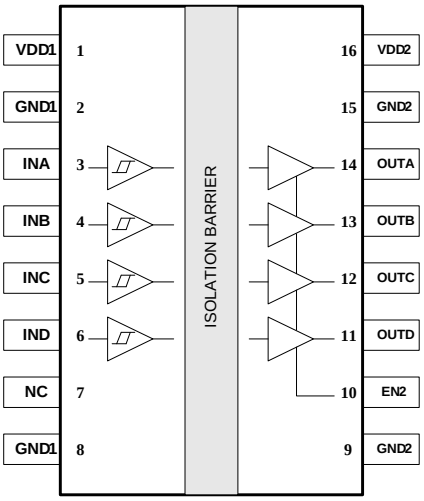


Figure 1. CMT8040x Pin List

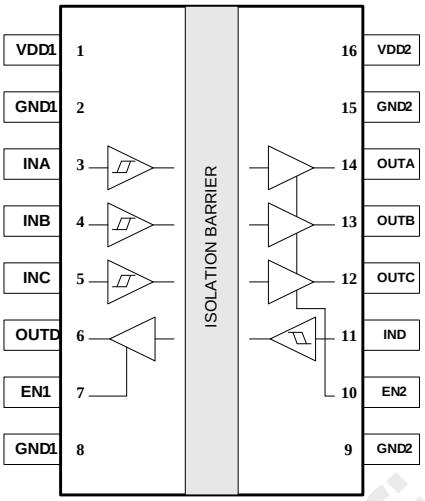


Figure 2. CMT8041x Pin List

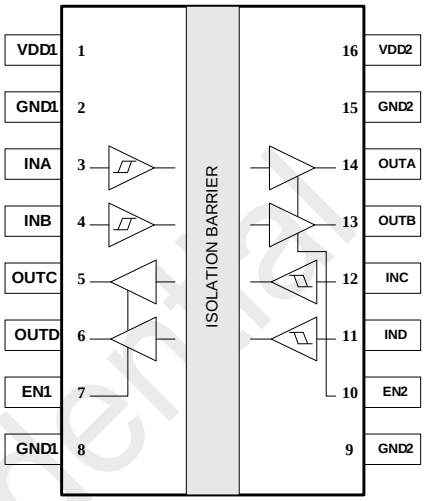


Figure 3. CMT8042x Pin List

Table 4. CMT8040 / 41 / 42x Pin Description

Pin Name	Pin Number			Description
	CMT8040	CMT8041	CMT8042	
VDD1	1	1	1	Power supply for isolator side 1
GND1	2	2	2	The ground reference for isolator side 1
INA	3	3	3	Input, channel A
INB	4	4	4	Input, channel B
INC	5	5	12	Input, channel C
IND	6	11	11	Input, channel D
NC / EN1	7	7	7	No connection for CMT8040x. Input, side 1 output enable for both CMT8041/42x, active logic high. When EN1 is high or NC, the outputs of side 1 are enabled. When EN1 is low, the outputs of side 1 are disabled to high impedance state
GND1	8	8	8	Ground 1, the ground reference for isolator side 1
GND2	9	9	9	Ground 2, the ground reference for isolator side 2
EN2	10	10	10	Input, side 2 output enable, active logic high. When EN2 is high or NC, the outputs of side 2 are enabled. When EN2 is low, the outputs of side 2 are disabled to high impedance state
OUTD	11	6	6	Output, channel D
OUTC	12	12	5	Output, channel C
OUTB	13	13	13	Output, channel B
OUTA	14	14	14	Output, channel A
GND2	15	15	15	Ground 2, the ground reference for isolator side 2
VDD2	16	16	16	Power supply for isolator side 2

8 Typical Application

8.1 Typical Application Schematic

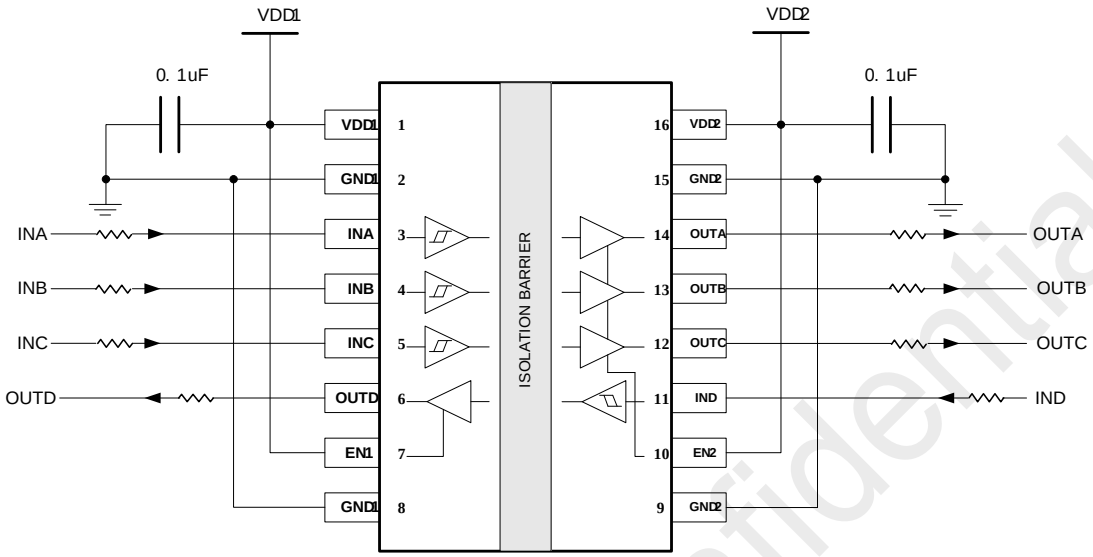


Figure 4. Typical Application Schematic (Take the CMT8041x as an example)

Note: *users should be careful not to connect ground and VDD reversely.*

8.2 PCB Layout Guidelines

The CMT804x requires a 0.1 µF bypass capacitor in both input side and output side. The capacitor should be placed as close as possible to the package pin of VDD1 and VDD2 respectively. The figures below show the recommended PCB layout. Please make sure the space under the chip keeps free from planes, traces, pads and via. To enhance the robustness of design, users may also include resistors (50 ~ 300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω ± 40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

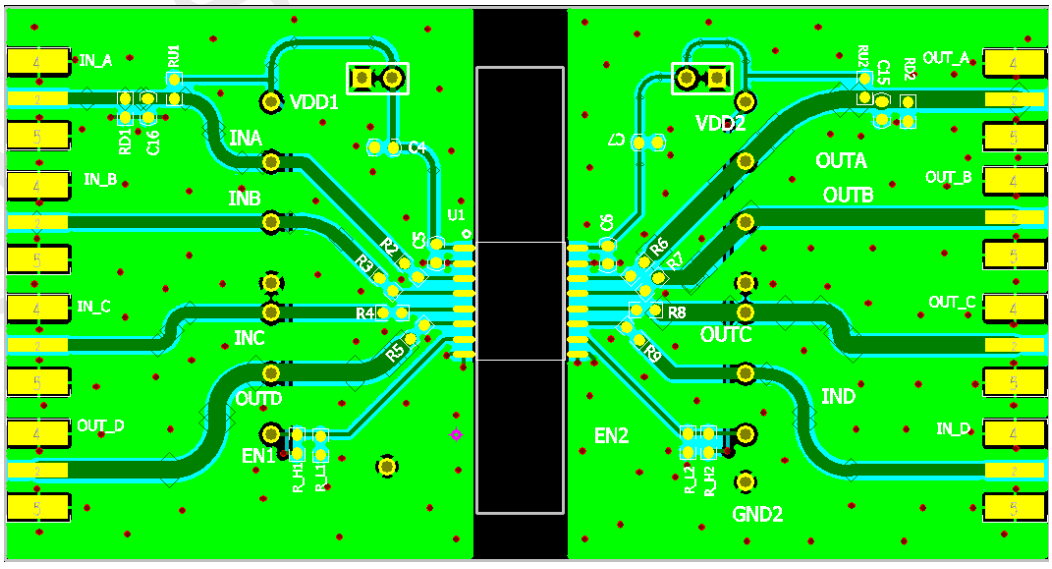


Figure 5. Recommended PCB Layout

9 Parameter Measurement Circuit Setup

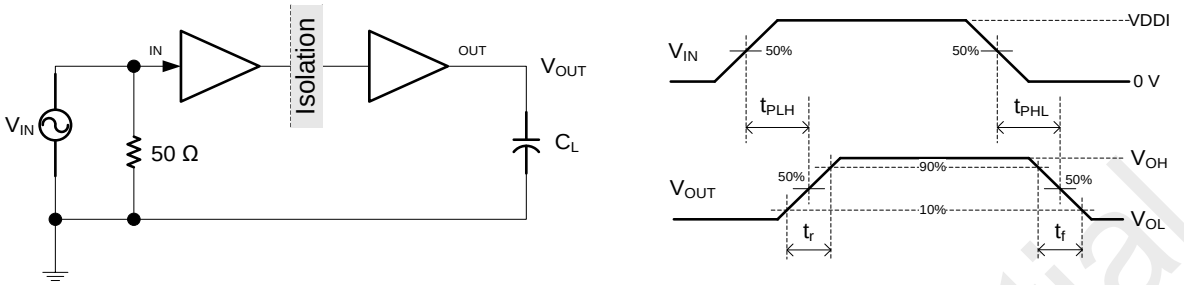


Figure 6. Switching Characteristics Test Circuit and Voltage Waveforms

Notes:

1. The input pulse is supplied by a generator V_{IN} having the following characteristics: f_{PULSE} ≤ 100 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. Load capacitance influences the measurement results quite a lot, including instrumentation and fixture capacitance, totally no more than 15 pF loading is preferred.

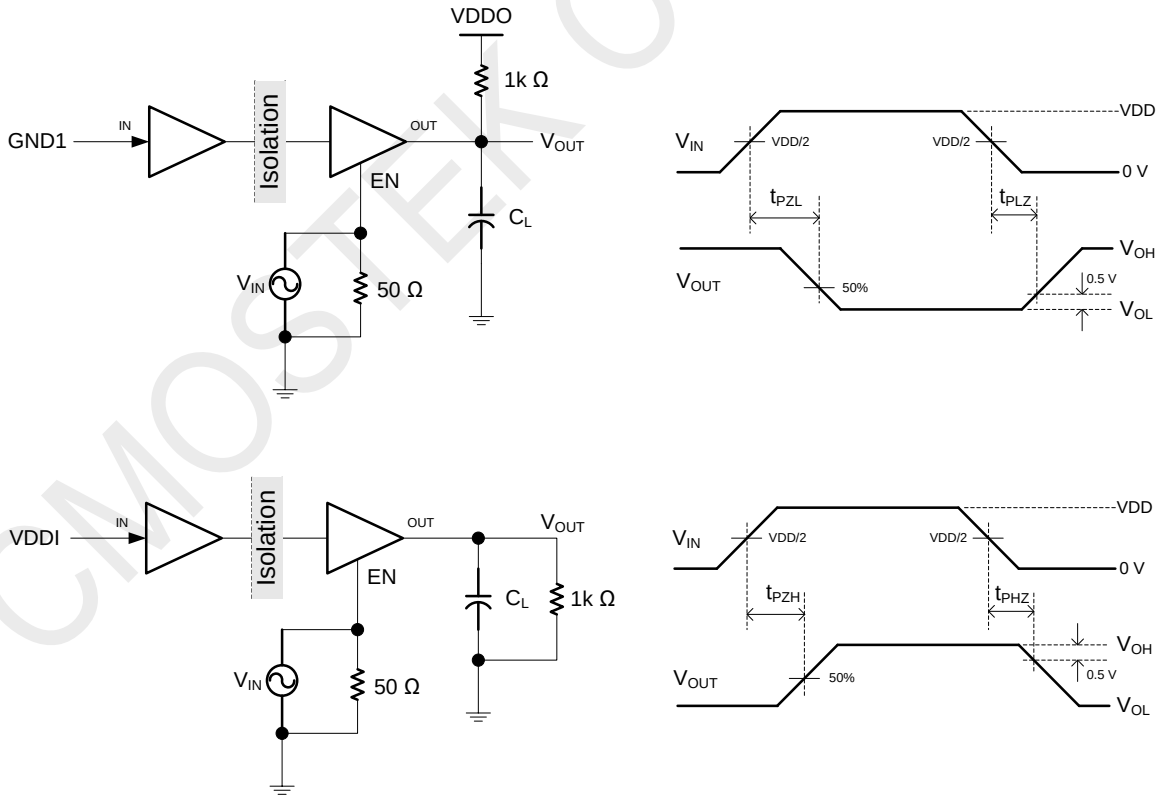


Figure 7. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Notes:

1. The input pulse is supplied by a generator having the following characteristics: f_{PULSE} ≤ 10 kHz, 50% duty cycle, tr ≤ 3 ns, tf ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

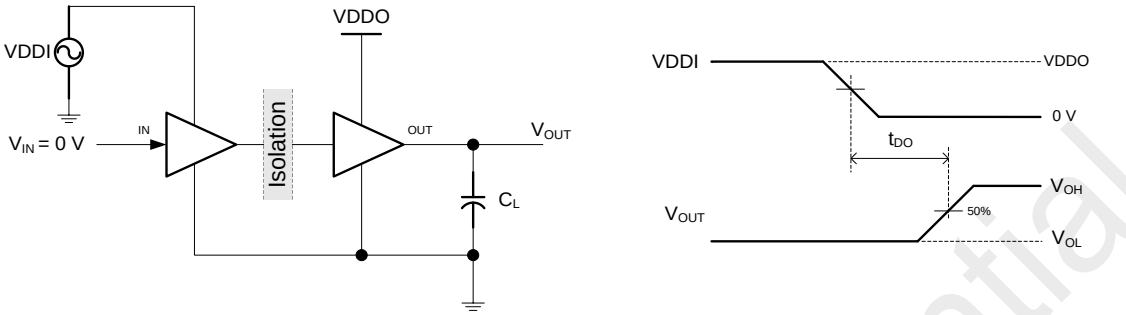


Figure 8. Default Output Delay Time Test Circuit and Voltage Waveforms

Notes:

1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
2. Power supply ramp rate = 10 mV/ns.

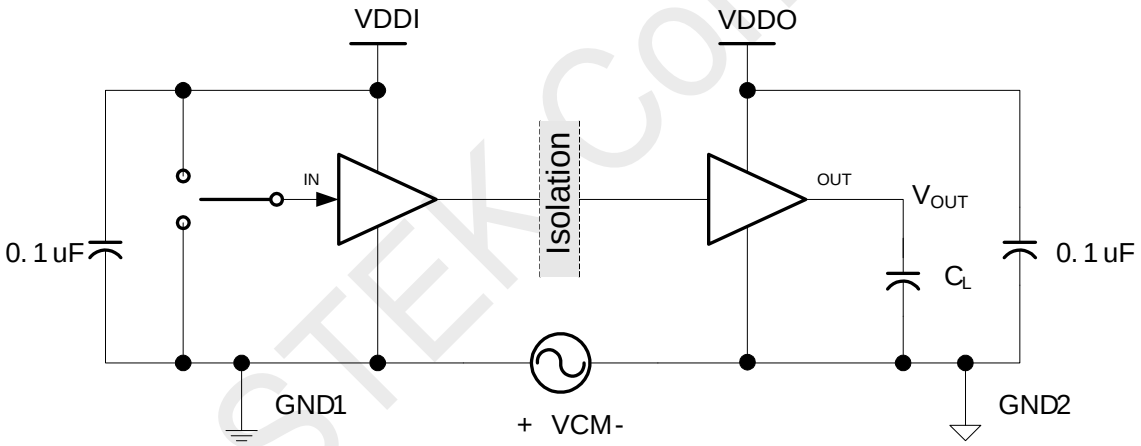


Figure 9. Common-Mode Transient Immunity Test Circuit

Notes:

1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

10 Electrical Specifications

10.1 Electrical Characteristics with 5 V Supply

VDD1 =VDD2= 5V, T_A= -40 to 125 ℃.

Table 5. Electrical Characteristics with 5 V Supply

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Poweron reset	V_{POR}	POR threshold as during power- up		2.3		V
	V_{HYS}	POR threshold hysteresis		0.1		V
Input threshold	V_{IT}	Input threshold at rising edge		1.6		V
	V_{ITHYS}	Input threshold hysteresis		0.4		V
High level input voltage	V_{IH}		2			V
Low level input voltage	V_{IL}				0.8	V
High level output voltage	V_{OH}	I_{OH} =-4mA	VDD- 0.3			V
Low level output voltage	V_{OL}	I_{OL} = 4mA			0.3	V
Output impedance	R_O			50		Ω
Input pull high or low current	Ipull			3	15	uA
Start-up time after POR	trbs			60		us
Common mode transient	CMTI		100		150	kV/us

10.2 Supply Current Characteristics with 5 V Supply

VDD1 = VDD2 = 5V, T_A= -40 to 125 ℃.

Table 6. Supply Current Characteristics with 5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8040x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	0.91		mA
	I_{DD2}	2.53		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.98		mA
	I_{DD2}	2.61		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.98		mA
	I_{DD2}	2.77		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.06		mA
	I_{DD2}	4.51		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.43		mA
	I_{DD2}	20.83		mA
CMT8041x				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	1.49		mA
	I_{DD2}	2.55		mA

Parameter	Symbol	Typ.	Max.	Unit
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.34		mA
	I_{DD2}	2.59		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.12		mA
	I_{DD2}	3.39		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.09		mA
	I_{DD2}	6.27		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	13.24		mA
	I_{DD2}	32.90		mA
CMT8042x				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	1.94		mA
	I_{DD2}	1.98		mA
Supply current: device is disabled. EN = VDDI, V_{IN} =VDDI,	I_{DD1}	3.99		mA
	I_{DD2}	4.07		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.04		mA
	I_{DD2}	3.13		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.82		mA
	I_{DD2}	3.91		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	6.74		mA
	I_{DD2}	12.60		mA

Table 7-1. Supply Current with 5 V Supply- Characteristics of CMT804x

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, C_L = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, C_L = 15 pF		9.1		ns
Propagation delay falling	t_{PHL}	See figure 6, C_L = 15 pF		7.8		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, C_L = 15 pF		1.2		ns
Rising time	tr	See figure 6, C_L = 15 pF		0.91		ns
Falling time	tf	See figure 6, C_L = 15 pF		0.89		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel delay Skew	t_{SK}(c2c)			0.6		ns
Part-to-part delay skew	t_{SK}(p2p)					ns
Disable high to tri-State	t_{PHZ}	See figure 7, C_L = 15pF, R_L=1k		10.55		ns
Enable to data high valid	t_{PZH}	See figure 7, C_L = 15pF, R_L=1k		12.4		ns
Disable low to tri-state	t_{PLZ}	See figure 7, C_L = 15pF, R_L=1k		24.05		ns
Enable to data low valid	t_{PZL}	See figure 7, C_L = 15pF, R_L=1k		25.3		ns

10.3 Supply Current Characteristics with 3.3 V Supply

VDD1 = VDD2 = 3.3V, T_A= -40 to 125 ℃.

Table 8. Supply Current Characteristics with 3.3 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8040x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	0.91		mA
	I_{DD2}	2.52		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.98		mA
	I_{DD2}	2.61		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.97		mA
	I_{DD2}	2.78		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.07		mA
	I_{DD2}	4.59		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.41		mA
	I_{DD2}	20.85		mA
CMT8041x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.47		mA
	I_{DD2}	2.53		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.45		mA
	I_{DD2}	2.62		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.07		mA
	I_{DD2}	3.19		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.72		mA
	I_{DD2}	5.00		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	10.51		mA
	I_{DD2}	22.86		mA
CMT8042x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.95		mA
	I_{DD2}	1.99		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.01		mA
	I_{DD2}	4.09		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.08		mA
	I_{DD2}	3.17		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	4.04		mA
	I_{DD2}	4.36		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	14.60		mA
	I_{DD2}	15.46		mA

Table 9-1. Supply Current with 3.3 V Supply - Characteristics of CMT804x

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, C_L = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, C_L = 15 pF		9.15		ns
Propagation delay falling	t_{PHL}	See figure 6, C_L = 15 pF		7.8		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, C_L = 15 pF		1.35		ns
Rising time	tr	See figure 6, C_L = 15 pF		1.01		ns
Falling time	tf	See figure 6, C_L = 15 pF		1.05		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel Delay Skew	t_{SK}(c2c)			0.8		ns
Part-to-part delay skew	t_{SK}(p2p)					ns
Disable high to tri-State	t_{PHZ}	See figure 7, C_L = 15pF, R_L=1k		15.25		ns
Enable to data high valid	t_{PZH}	See figure 7, C_L = 15pF, R_L=1k		20		ns
Disable low to tri-state	t_{PLZ}	See figure 7, C_L = 15pF, R_L=1k		27.65		ns
Enable to data low valid	t_{PZL}	See figure 7, C_L = 15pF, R_L=1k		30.15		ns

10.4 Supply Current Characteristics with 2.5 V Supply

VDD1 = VDD2 = 2.5 V, T_A= -40 to 125 ℃.

Table 10. Supply Current Characteristics with 2.5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8040x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	0.90		mA
	I_{DD2}	2.52		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.98		mA
	I_{DD2}	2.61		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.97		mA
	I_{DD2}	2.78		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.06		mA
	I_{DD2}	4.59		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.41		mA
	I_{DD2}	20.85		mA
CMT8041x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.41		mA
	I_{DD2}	2.49		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	4.43		mA
	I_{DD2}	2.60		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	2.91		mA
	I_{DD2}	3.16		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.43		mA
	I_{DD2}	4.53		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	7.91		mA
	I_{DD2}	18.80		mA
CMT8042x				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.94		mA
	I_{DD2}	1.98		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	3.99		mA
	I_{DD2}	4.07		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.04		mA
	I_{DD2}	3.12		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	3.82		mA
	I_{DD2}	3.91		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	6.74		mA
	I_{DD2}	12.60		mA

Table 11-1. Supply Current with 2.5 V Supply - Characteristics of CMT804x

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR			150		Mbps
Minimum pulse width	PW	See figure 6, C_L = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, C_L = 15 pF		9.3		ns
Propagation delay falling	t_{PHL}	See figure 6, C_L = 15 pF		7.75		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, C_L = 15 pF		1.55		ns
Rising time	tr	See figure 6, C_L = 15 pF		1.04		ns
Falling time	tf	See figure 6, C_L = 15 pF		1.23		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel Delay Skew	t_{SK}(c2c)			0.7		ns
Part-to-part delay skew	t_{SK}(p2p)			0		ns
Disable high to tri-State	t_{PHZ}	See figure 7, C_L = 15pF, R_L=1k		21.25		ns
Enable to data high valid	t_{PZH}	See figure 7, C_L = 15pF, R_L=1k		26.95		ns
Disable low to tri-state	t_{PLZ}	See figure 7, C_L = 15pF, R_L=1k		29.4		ns
Enable to data high valid	t_{PZL}	See figure 7, C_L = 15pF, R_L=1k		33.05		ns

10.5 Typical Characteristics

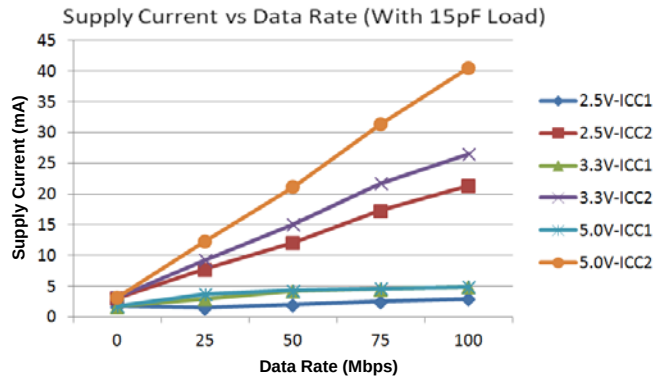


Figure 9-1. Supply Current vs. Data Rate (with 15-pF Load) T_A=25℃ C_L=15pF

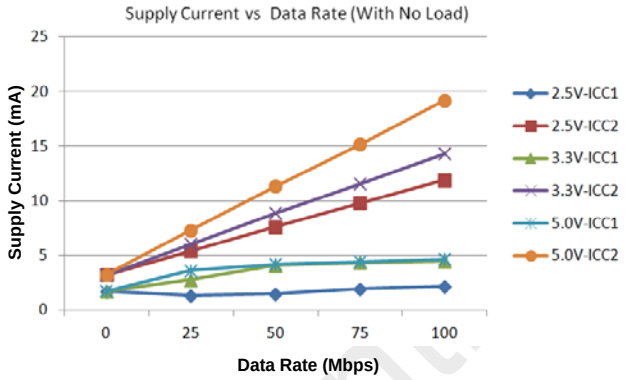


Figure 9-2. Supply Current vs. Data Rate (with No Load) T_A=25℃ C_L=No Load

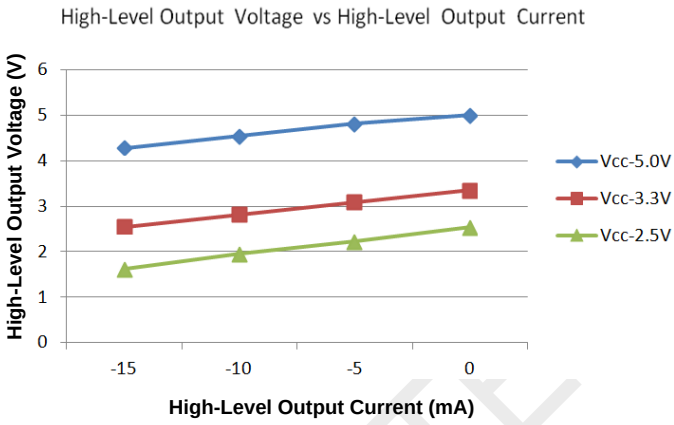


Figure 9-3. High-Level Output Voltage vs. High-Level Output Current (T_A=25℃)

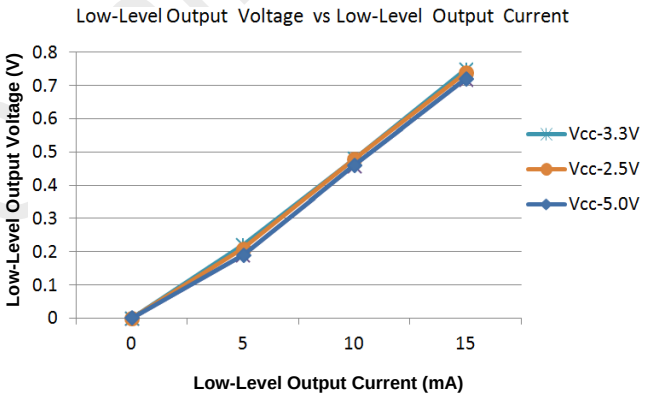


Figure 9-4. Low-Level Output Voltage vs. Low-Level Output Current(T_A=25℃)

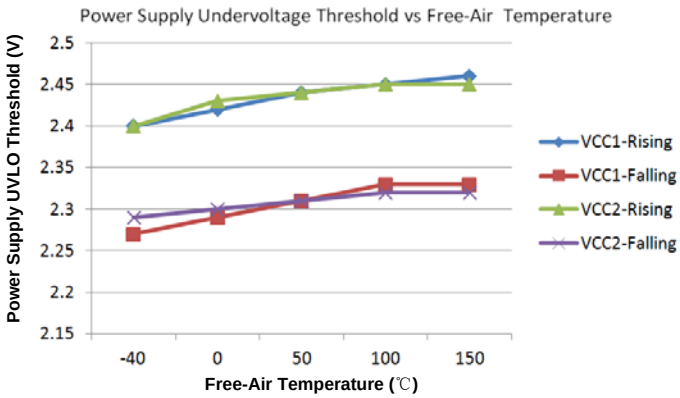


Figure 9-5. Power Supply Under-voltage Threshold vs. Free-Air Temperature

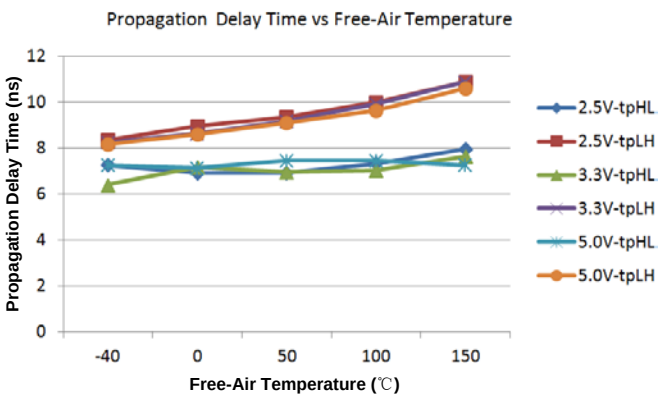


Figure 9-6. Propagation Delay Time vs. Free-Air Temperature

10.6 Insulation Specifications

Table 12. Insulation Specifications

Parameters	Sym.	Condition	Value		Unit
			NB SOIC-16	WB SOIC-16	
External clearance[1]	CLR	The shortest terminal-to-terminal distance through air	4.0	8.0	mm
External creepage[1]	CRP	The shortest terminal-to-terminal distance across the package surface	4.0	8.0	mm
Distance through insulation	DTI	Minimum internal gap	> 25	> 25	um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11);IEC 60112	> 400	> 400	V
Material group	-		II	II	-
Overvoltage category per IEC 60664-1	-	Rated mains voltage ⩽ 300 V_{RMS}	I	I	-
		Rated mains voltage ⩽ 600 V_{RMS}	I-IV	I-IV	-
		Rated mains voltage ⩽ 1000 V_{RMS}	I-III	I-III	-
DIN VDE V 0884-11:2017-01[2]					
Maximum repetitive isolation voltage	V_{IORM}		565	1414	V_{pk}
Maximum isolation working voltage	V_{IOWM}	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) test		1000	V_{RMS}
		DC voltage		1414	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM},t = 60 s (qualification); t = 1 s (100% production)	5300	7000	V_{pk}
Maximum surge isolation voltage[3]	V_{IOSM}	Test method per IEC60065, 1.2/50 us waveform, V_{TEST} = 1.6 x V_{IOSM} (qualification)	5300	7000	V_{pk}
Apparent charge[4]	q_{pd}	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s		1696	⩽5pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s		2262	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s		2651	
Isolation capacitance, input to output[5]	C_{IO}	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	0.8	0.8	pF
Isolation resistance, input to output[5]	R_{IO}	V_{IO} = 500 V	$>10^{10}$	$>10^{10}$	Ω
UL 1577					
Withstand isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)		5000	V_{RMS}

Notes:

[1]. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

[2]. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

[3]. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

[4]. Apparent charge is electrical discharge caused by a partial discharge (pd).

[5]. All pins on each side of the barrier are tied together creating a two-terminal device.

10.7 Safety-related Certifications

Table 13. Safety-related Certifications

VDE	CSA	UL	CQC	TUV
DIN VDE V0884-11:2017-01 （Patents pending）	IEC 60950-1, IEC 62368-1 and IEC 61010-1 （Patents pending）	Recognized under UL 1577 Component Recognition Program （Patents pending）	GB 4943.1-2011 （Patents pending）	EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2: 2013 （Patents pending）
Certificate number: pending	Master contract number: pending	File number: pending	Certificate number: pending	Client ID number: pending

10.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures

Table 14. Safety Limiting Values

Parameters	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-16	
Safety input, output, or supply current	Is	$R_{\theta JA}$ = 140 °C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C	160		mA
		$R_{\theta JA}$ = 84 °C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C		237	mA
Total power dissipation at 25℃	Ps			1499	W
Case temperature	Ts		125	125	℃

10.9 Thermal Information

Table 15. Thermal Information

Parameter	Symbol	Value		Unit
		NB SOIC-16	WB SOIC-16	
Junction-to-ambient thermal resistance	θ_{JA}	78.9	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	41.1	41.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	49.5	43.6	°C/W

11 Function Description

11.1 Function Overview

The CMT804x device is a high-performance, quad-channel digital isolator with 5000 V_{RMS} isolation ratings .The CMT804x has an On-Off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The CMT804x also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The figure below shows a conceptual detail of how the On-Off keying scheme works.

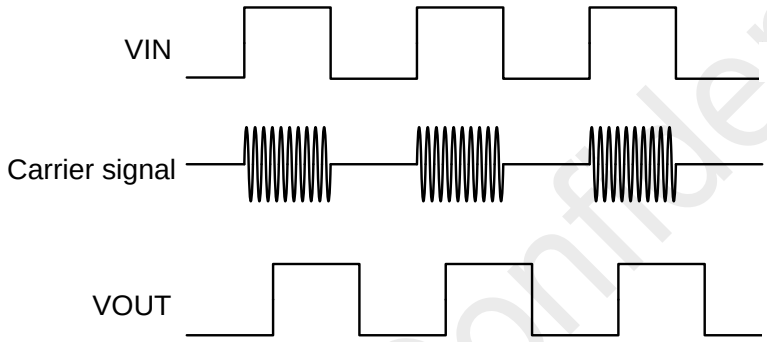


Figure 10. On-Off Keying Based Modulation Scheme

11.2 Functional Modes

The table below lists the functional modes of the CMT804x.

Table 16. Function Table[1]

V_{DD1}	V_{DD2}	Input (INx)[2]	Output Enable (ENx)	Output (OUTx)	Comment
PU	PU	H	H or open	H	Normal operation: A channel output assumes the logic state of its input
		L	H or open	L	
		Open	H or open	Default	Default mode: when INx is open, the corresponding channel output goes to its default logic state
X	PU	X	L	Z	A low value of output enable causes the outputs to be high impedance
PD	PU	X	H or open	Default	Default mode: when VDDI is unpowered, a channel output assumes the logic state based on the selected default option. When VDD1 transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When VDD1 transitions from powered-up to unpowered, channel output assumes the selected default state
X	PD	X	X	Undetermined	When VDD2 is unpowered, a channel output is undetermined[3]. When VDD2 transitions from unpowered to powered-up, a channel output assumes the logic state of the input

Notes:

[1]. VDDI = Input-side VDD; VDD2 = output-side VDD; PU = Powered up (VDD ≥ 2.6 V); PD = Powered down (VDD ≤ 1.7 V); X = Irrelevant; H= High level; L = Low level; Z = High Impedance.

[2]. A strongly driven input signal can weakly power the floating VDD through an internal protection diode and cause undetermined output.

[3]. The outputs are in undetermined state when 1.7 V < VDD1, VDD2< 2.6V.

11.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See the figure below for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

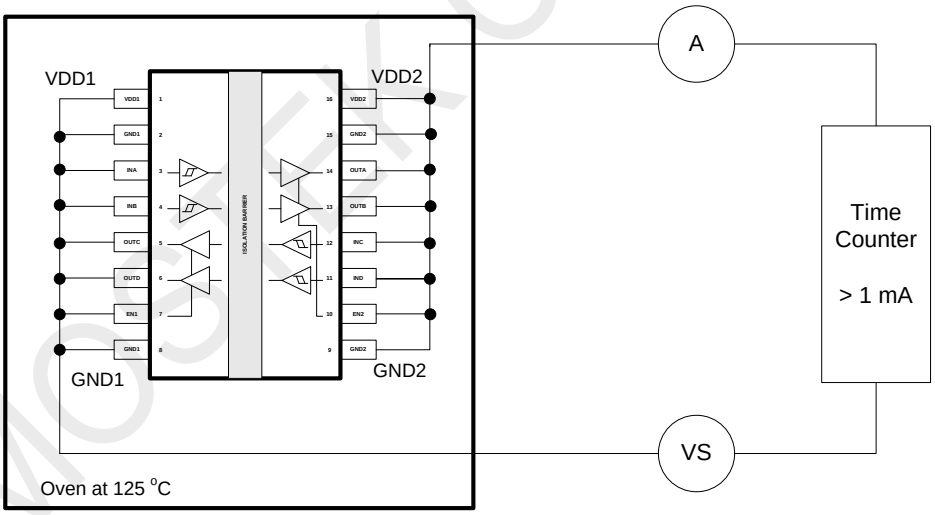


Figure 11. Test Setup for Insulation Lifetime Measurement

12 Packaging Information

The packaging information of the CMT804x SOIC16 is shown in the figures below.

12.1 CMT804x Narrow Body SOIC-16 Packaging

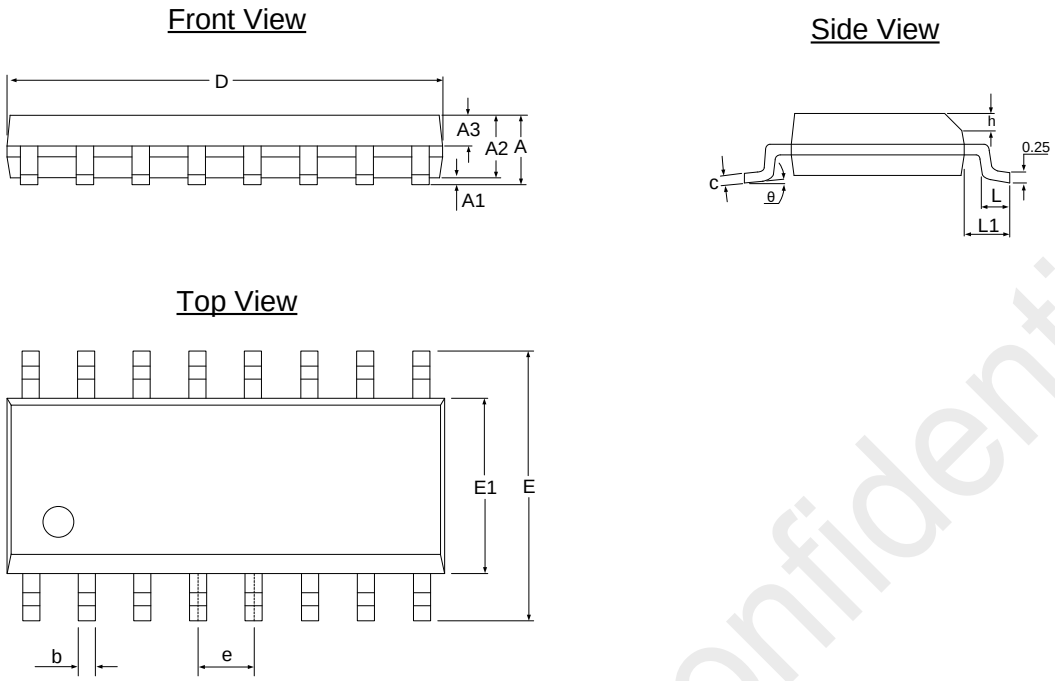


Figure 12. Narrow Body SOIC-16 Packaging

Table 17.Narrow Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
b	0.36	-	0.49
c	0.19	-	0.25
D	9.80	9.90	10.0
E	5.80	-	6.20
E1	3.80	3.90	4.00
e	1.27		
L	0.40	-	1.00
L1	1.05		
θ	0	-	8°

12.2 CMT804x Wide Body SOIC-16 Packaging

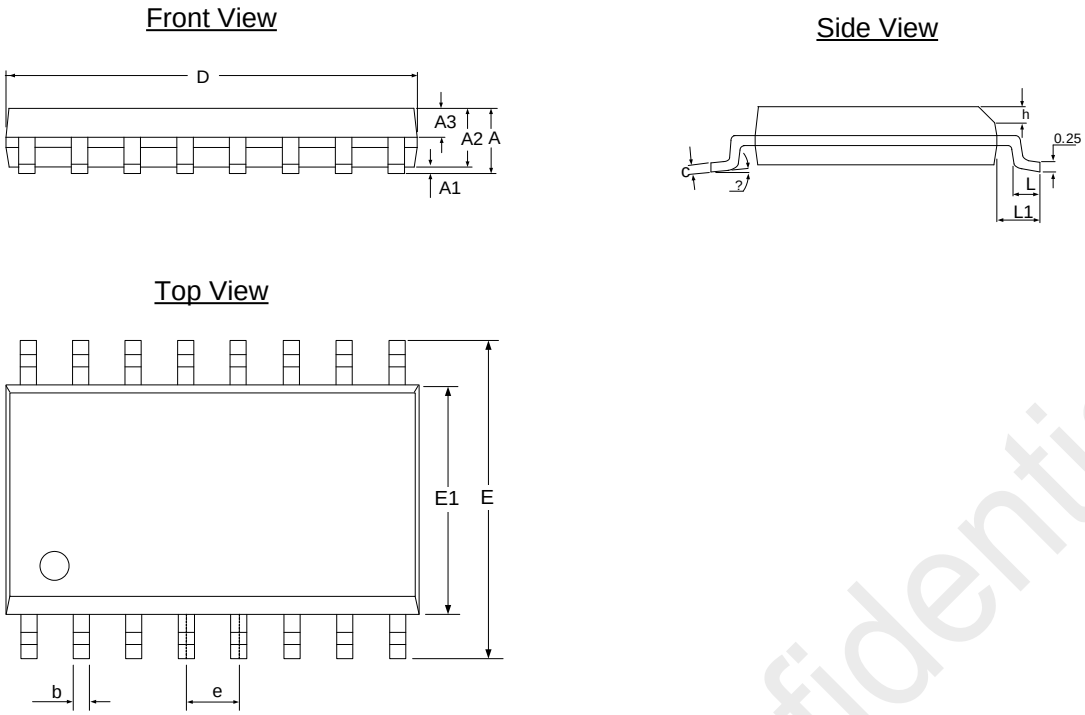


Figure 13. Wide Body SOIC-16 Packaging

Table 18. Wide Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1	1.40		
θ	0	-	8°

13 Top Marking

Figure 14. CMT804x Top Marking

Table 19. CMT804x Top Marking Information

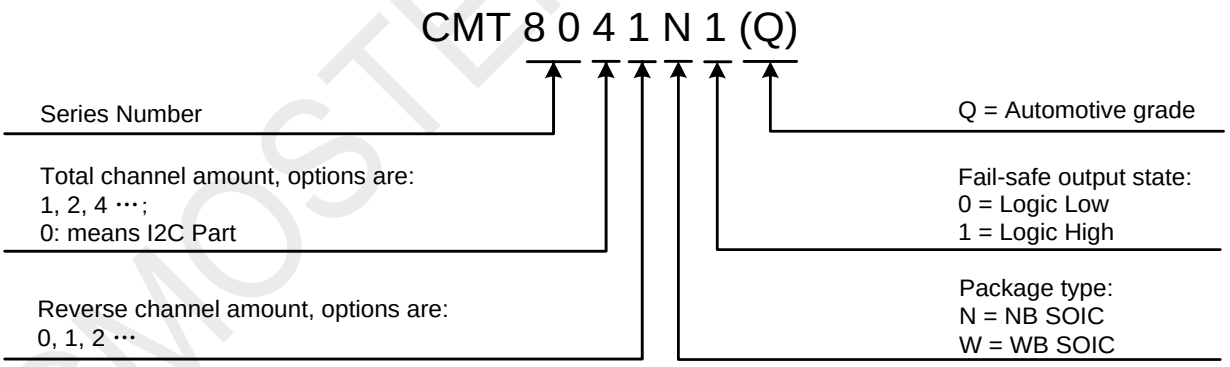
Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.5 mm, align right
Line 1 Marking	P = 0 / 1 / 2, refers to part number CMT8040x / CMT8041x / CMT8042x respectively. NNN is the last characters following CMT804x in part number naming. See Chapter 14 Part number naming rule for details
Line 2 Marking	The date code is assigned by the package factory. YY is the last 2 digits of the year. WW is the working week. ①②③④⑤⑥ is internal trace code

14 Ordering Information

Table 20. Part Number List

Part Number	Isolation Rating (kV)	Number of Total Channels	Number of Reversed Channels	Max Data Rate (Mbps)	Default Output State	Automotive Grade	Package
CMT8040N0	3.75	4	0	150	Low	No	NB SOIC-16
CMT8040N1	3.75	4	0	150	High	No	NB SOIC-16
CMT8041N0	3.75	4	1	150	Low	No	NB SOIC-16
CMT8041N1	3.75	4	1	150	High	No	NB SOIC-16
CMT8042N0	3.75	4	2	150	Low	No	NB SOIC-16
CMT8042N1	3.75	4	2	150	High	No	NB SOIC-16
CMT8040W0	5	4	0	150	Low	No	WB SOIC-16
CMT8040W1	5	4	0	150	High	No	WB SOIC-16
CMT8041W0	5	4	1	150	Low	No	WB SOIC-16
CMT8041W1	5	4	1	150	High	No	WB SOIC-16
CMT8042W0	5	4	2	150	Low	No	WB SOIC-16
CMT8042W1	5	4	2	150	High	No	WB SOIC-16

Part Number Naming Rule:



Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

15 Revise History

Table 21. Revise History Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2021/09/01
0.2	10	Update the supply current characteristic data	2022/09/01
0.3	10.6	Update the data of withstand voltage	2022/09/05

16 Contacts

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