NuMicro® Family
Arm® 32-bit Cortex®-M23 Microcontroller

M2354 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro® M2354 Series is a TrustZone® for Armv8-M architecture empowered microcontroller series focusing on IoT Security based on Arm® Cortex®-M23 CPU core technology. It runs up to 96 MHz with 1024 Kbytes embedded Flash memory and 256 Kbytes SRAM, supporting Flash in dual-bank mode, secure firmware OTA (Over-The-Air) update, ultra-low power consumption in normal run with 89.3 uA/MHz in LDO mode, 39.6 uA/MHz in DC-DC mode and an 8x40 COM/SEG LCD driver inside. Besides the fundamental microcontroller security features, it further enhances the chip-level security in covering side-channel attacks mitigation to crypto hardware engine, fault injection mitigation for operating voltage and clock as well as active shield to cryptographic key storage. The series supports power supply voltage from 1.7V ~ 3.6V in operating temperature range from -40°C to +105°C, and is equipped with both LDO and DC-DC power supply functionalities. The M2354 Series is quite competitive for those devices that need more secure, fast computing and low power in the IoT market.

The one of major challenges for IoT devices that are connected to cloud services or other devices by network communication is security, so the IoT devices must meet some security requirements to protect firmware, software and secure assets from being stolen or modified by an attacker. "**Execution**", "**Storage**", and "**Connectivity**" are the three important security targets for IoT devices.

The TrustZone® technology based on Armv8-M architecture is a System-on-Chip (SoC) and CPU system-wide approach to microcontroller security. The whole system isolates secure and normal worlds to avoid the trusted assets being accessed by a non-secure process. In addition to the firmware-level security, the M2354 series is also equipped with rich functions to improve system security. The Secure Bootloader supports trusted system-boot feature which can protect certificated firmware from being replaced with malware possibly in the upgrade processing and taking control of system resource finally. The hardware crypto accelerators, including AES, ECC and RSA, support encryption and decryption operations to offload the main processor's computing power and ensure data transmission in secure.

The M2354 series also enhances firmware update security requirement with monotonic version counter. The firmware cannot be rollback to older one which has lower security protection. Furthermore, there is a secure crypto keys storage protected by the chip-level active shield function to physical intrusion. The series addresses the physical attack protection and system security certification for Arm® PSA Certified™ Level 2 even for PSA Certified™ Level 3.

Other than security, low power is also vital for IoT applications. The M2354 series supports 4 core power levels with both LDO and DC-DC power supply mechanism. Except normal run mode, the series also provides idle run mode with power consumption 31.5 µA/MHz in LDO mode and 14.3 µA/MHz in DC-DC mode. The current consumption of Deep Power-Down mode without V_{BAT} is less than 0.1 µA.

The M2354 series is equipped with plenty of peripherals such as Timers, Watchdog Timers, RTC, PDMA, UART, Universal Serial Control Interface (USCI), SPI/ I²S, I^2C, GPIOs, makes it highly suitable for connecting comprehensive external modules. The M2354 integrates high performance analog front-end circuit blocks, such as 16 channels of 12-bit 6 MSPS ADC, temperature sensor, low voltage reset (LVR) and brown-out detector (BOD) to enhance product performance, reduce external components and form factor simultaneously. Moreover, it supports up to 8x40 COM/SEG for segment LCD display needed such as metering devices.

The M2354 series provides LQFP48 (7mm x 7mm), LQFP64 (7mm x 7mm) and LQFP128 (14mm x 14mm).

The NuMicro® M2354 is suitable for a wide range of applications such as:

- IoT Devices with Secure Connection
- Collaborative Secure Software Development Business Model
- Secure Fingerprint Lock
- Smart Home Appliance

- Smart City Facilities
- Wireless Sensor Node Device (WSND)
- Secure Wireless Connectivity Module (SWCM)
- Auto Meter Reading (AMR)
- Digital Currency Authentication
- Trusted Execution Environment (TEE) with Trusted Applications (TAs)

2 FEATURES

Core And System	
Arm® Cortex®-M23	• Arm® Cortex®-M23 processor, running up to 96 MHz • 96 MHz at 1.8V-3.63V; 84 MHz at 1.7V • Supports Arm® TrustZone® Technology • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Security Attribution Unit (SAU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Built-in Embedded Trace Macrocell (ETM) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmable and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Secure Configuration Unit (SCU)	• Configure SRAM's security and privilege attribution block by block • Configure GPIOs' security and privilege attribution port by port • Configure peripherals' security and privilege attribution • Generates secure and privilege violation interrupt • Equipped with a 24-bit timer as a non-secure state monitor • Monotonic firmware version counter • Debug protection mechanism • Product life-cycle management
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V)
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Power Manager	• Dual voltage regulator is available for DC-DC converter or LDO • Supports 1.26V, 1.2V, 1.1V and 0.9V core voltage while operating • Supports Power-down mode • Supports Standby Power -down mode • Supports Low Leakage Power-down mode • Supports Ultra-low Leakage Power-down mode • Supports Fast Wake-up Power-down mode • Supports Deep Power-down mode

Security	• 128-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • One built-in temperature sensor with 1°C resolution
Memories	
Boot Loader	• Factory pre-loaded 16 KB mask ROM for secure boot procedure • Uses SHA-256 and ECC-256 to validate data in APROM, LDROM and external SPI Flash • Nuvoton ISP (In-System-Programming) tool for firmware upgrade via UART and high speed USB device • ISP/IAP libraries
Flash	• Dual bank 1024/512KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade • 16 KB on-chip Flash for user-defined loader (LDROM) • Excute Only Memory (XOM) for intelectual property protection • All on-chip Flash support 2 KB page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Always boot from boot loader • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 256 KB on-chip SRAM includes: – 32 KB SRAM located in bank 0 that supports hardware parity check; Exception (NMI) generated upon a parity check error • 128/128 KB SRAM located in bank 1 and bank2 • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation

Peripheral DMA (PDMA)	• 16 independent and configurable channels for automatic data transfer between memories and peripherals • 8 channels of PDMA1 can be configured as secure or non-secure channels • Supports time-out function when transfer time-out • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed external crystal oscillator (extLXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25% accuracy that can optionally be used as a system clock • 48 MHz High-speed Internal RC oscillator (HIRC48) trimmed to 0.25% accuracy that can optionally be used as a system clock • 32 kHz Low-speed Internal RC oscillator (LIRC32) for RTC function • Up to 200 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain • The RTC clock source includes Low-speed external crystal oscillator (extLXT) and 32 kHz Low-speed Internal RC oscillator (LIRC32) • The RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition

		• Supports 1 Hz clock output for calibration • Frequency of RTC clock source compensated by RTC_FRWQADJ register
Timers		
32-bit Timer	**TIMER**	• Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
	PWM	• Eight 16-bit PWM counters with 12-bit clock prescale with up to 64 MHz • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)		• Twelve 16-bit counters with 12-bit clock prescale for twelve 36 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC or DAC to start conversion
Basic PWM (BPWM)		• Two 16-bit counters with 12-bit clock prescale for twelve 36 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM

	output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit down counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 19-ch SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V • Two power saving modes: Power-down mode and Standby mode. • Supports calibration capability • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or EPWM trigger • Configurable EADC sampling time • Up to 19 sample modules • Double data buffers for sample module 0~3 • PDMA operation
Digital-to-Analog Converter (DAC)	• Two 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time • Maximum output voltage AV_{DD} -0.2V at buffer mode • Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software • Supports group mode for synchronized data update of two DACs. • PDMA operation

Analog Comparator (ACMP)	• Two rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, DAC output, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports four programmable propagation speeds for power saving. • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
LCD	• Supports the following COM/SEG configurations: – 320 dots (8-COM x 40-SEG) – 252 dots (6-COM x 42-SEG) – 176 dots (4-COM x 44-SEG) – 104 dots (8-COM x 13-SEG) for M2354SIFAE • Supports maximum 8 COM driving pins, multiplexed with GPIO pins • Supports maximum 44 SEG driving pins, multiplexed with GPIO pins • Supports 3 bias voltage levels 1/2, 1/3, and 1/4 • Supports 8 duty ratios 1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, and 1/8 • Supports clock frequency divider from 2, 4, 6… 2048 to configure the LCD operating frequency • Configurable frame counting event interrupt period • Supports LCD blinking display controlled by frame counting event. • Supports LCD frame end interrupt • LCD keeps display or blinking even if in Power-down mode when LCD clock source is selected as LIRC or LXT • Supports both type A and type B driving waveforms
Communication Interfaces	
Low-power UART	• Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1

		• Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation
Smart Card Interface		• Three sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I^2C		• Three sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
SPI/I^2S	**SPI**	• Up to four sets of SPI/I^2S controllers with Master/Slave mode • SPI/ I^2S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function

		• Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode • PDMA operation
	I²S	• Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
QSPI		• One set of SPI Quad controller with Master/Slave mode • 2-bit Transfer mode • Dual and Quad I/O Transfer mode • QSPI provides separate 8-level of 32-bit transmit and receive FIFO buffers • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • 3-wired, no slave select signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode • PDMA operation
I²S		• One set of I²S interface with Master/Slave mode • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Universal Serial Control Interface (USCI)		• Two sets of USCI, configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode
	UART	• Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and

	programmable flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports wake-up function • PDMA operation **SPI** • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function by slave select signal in slave mode • Supports one data channel half-duplex transfer • PDMA operation **I^2C** • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data payload • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps) • Supports 10-bit mode • Supports 10-bit bus time out capability • Supports bus monitor mode • Supports power-down wake-up by data toggle or address match • Supports multiple address recognition • Supports device address flag • Programmable setup/hold time
Controller Area Network (CAN)	• Two sets of CAN 2.0B controllers • Each supports 32 Message Objects; each Message Object has its own identifier mask • Programmable FIFO mode (concatenation of Message Object) • Disabled Automatic Re-transmission mode for Time Triggered CAN applications • Supports power-down wake-up function
Secure Digital Host Controller (SDHC)	• One sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0

	• Supports 36 MHz to achieve 192 Mbps at 3.3V operation • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space • 8-/16-bit data width • Supports byte write in 16-bit data width mode • Supports variable external bus base clock (MCLK) which based on HCLK • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode • Supports LCD interface i80 mode • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O. • Improve access efficiency by using single cycle I/O bus
Control Interfaces	
Quadrature Encoder Interface (QEI)	• Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP
Enhanced Capture (ECAP)	• Input Capture Timer/Counter • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports

	• Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 1.1 Host Controller** • Compliant with USB Revision 1.1 Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Supports port power control and port overcurrent detection • Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports suspend function when no bus activity existing for 3 ms • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1024 bytes configurable RAM for endpoint buffer • Remote wake-up capability
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports both prime field GF(p) and binary field GF(2m) • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes • Supports Curve25519 • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p) • Supports three techniques to improve side-channel attack

	protection ability • Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197 • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum • Supports SM4 cipher block alogrithm
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512 • Compliant with FIPS 180/180-2 • Supprots SM3 Cryptographic Hash Alogrithm
Rivest, Shamir and Adleman Cryptography (RSA)	• Hardware RSA accelerator • Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits • Supports Chinese Remainder Theorem (CRT) decryption with 2048, 3072 and 4096 bits • Supports three techniques to improve side-channel attack protection ability
Pseudo Random Number Generator (PRNG)	• Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits only generate for Key Store) • Able to take the true random number seed from TRNG
True Randon Number Generator (TRNG)	• Up to 800 random bits per second • Provide the true random number seed for PRNG
Key Store	
Key Store	• Supports programming interface for key management • Supports multiple key size from 128 bits to 4096 bits • Supports 4 Kbytes SRAM, 2 Kbytes Flash and 544bytes OTP for key storage • Supports 32 keys for SRAM, 32 keys for Flash and 8 keys for OTP at most • Supports crypto engine access or store key in key store directly • Supports ECDH operation with ECC and PRNG engine • Supports to store middle data for RSA CRT and SCAP mode • Supports revoke operation for each key • Supports erase key in SRAM/Flash and revoke key in OTP

	while tamper detected • Supports integrity checking • Supports data scrambling at SRAM, Flash and OTP • Supports data remanence prevention at SRAM • Supports silent access for side-channel protection at SRAM, Flash and OTP
Attack Detection	
Attack Detection (TAMPER)	• Includes voltage, clock and I/O tamper detectors: – Voltage: ◆ HV detector detects if V_{DD} › 4.0V ◆ LV detector detects if LDO_CAP 〉 ± 20% – Clock detector: ◆ detects if external clock (LXT) is failed or stopped – I/O tamper detector: ◆ detects GPF6~11 pins • Provides event response after an attack detected: – Clear key or data content in SRAM and Flash of Key Store, and revoke the OTP in Key Store – Clear RTC spare register – Reset Crypto – Chip reset – Interrupt – Wake up the system • Not supported in DPD mode.

3 PARTS INFORMATION

3.1 Package Type

Part No.	LQFP48	LQFP64	LQFP128
M2354	M2354LJFAE	M2354SJFAE	M2354KJFAE

3.2 M2354 Series Selection Guide

PART NUMBER			M2354					
			LJFAE		SJFAE		KJFAE	
Flash (KB)			1024		1024		1024	
SRAM (KB)			256		256		256	
ISP Loader ROM (KB)			16					
I/O			40		50		106	
32-bit Timer			4					
Tamper I/O			1		1		6	
RTC			√					
Connectivity	LPUART		6					
	ISO-7816		3					
	Quad SPI	SPI/I²S	1	3	1	4	1	4
	I²S		1					
	I²C		3					
	USCI (UART/I²C/SPI)		2					
	CAN		1					
	LIN		2					
	SDHC		1		1		1	
Crypto	TRNG		√					
	AES		√					
	ECC		√					
	SHA/HMAC		√					
	RSA		√					
Enhanced Security	FVC		√					
	DPM		√					
	PLM		√					
	Key Store		√					
Power Glitch Detector			√					
LCD (COMXSEG)			-		8 X 13		8 X 40	
16-bit Enhanced PWM			12					
16-bit Basic PWM			12					
QEI			2		2		2	
ECAP			1		1		1	
USB 2.0 FS OTG			√					
12-bit ADC			11		16		16	
12-bit DAC			2					
Analog Comparator			2		2		2	
External Bus Interface			√		√		√	
Package			LQFP48		LQFP 64		LQFP 128	

Table 3-1 M2354 Series Selection Guide

3.3 M2354 Series Selection Code

M23	54	K	J	F	A	E
Secure Core	Line	Package	Flash	SRAM	Rev.	Temperature
Cortex®-M23	54: Ultra Line (Segment LCD)	L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm) K: LQFP128 (14x14 mm)	J: 1024 KB	F: 256 kB		E: -40°C~105°C

Table 3-2 M2354 Series Selection Code

4 PIN CONFIGURATION

Users can find pin configuration information in the M2354 Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M2354 Pin Diagram

4.1.1.1 M2354 LQFP 48-Pin Diagram

Corresponding Part Number: M2354LJFAE

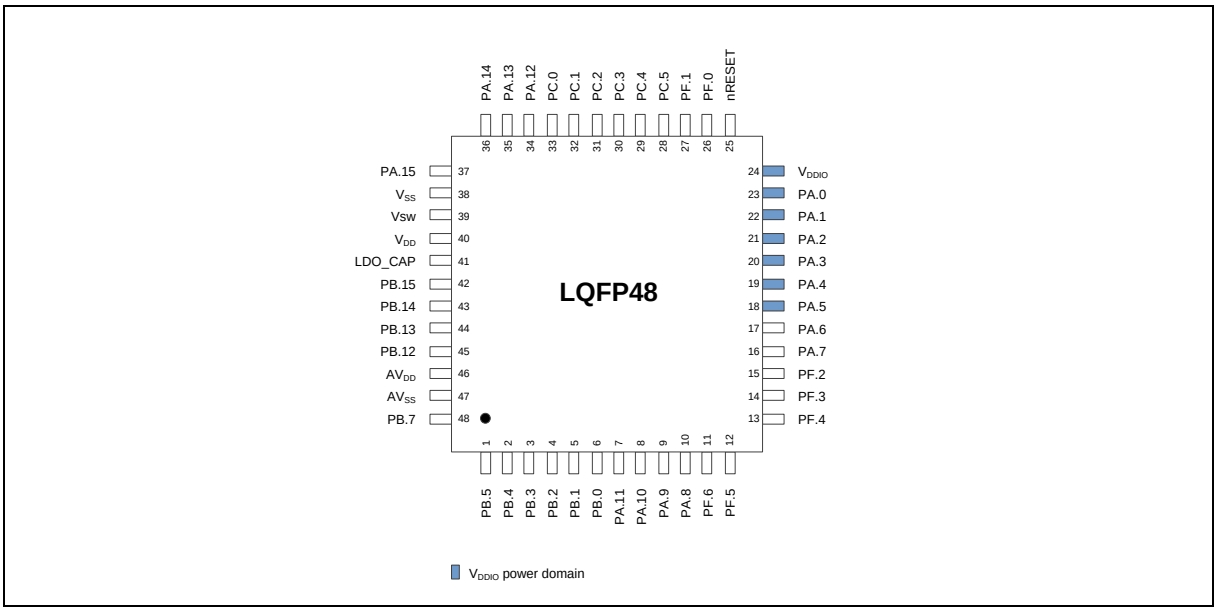


Figure 4.1-1 M2354 LQFP 48-pin Diagram

4.1.1.2 M2354 LQFP 64-Pin Diagram

Corresponding Part Number: M2354SJFAE

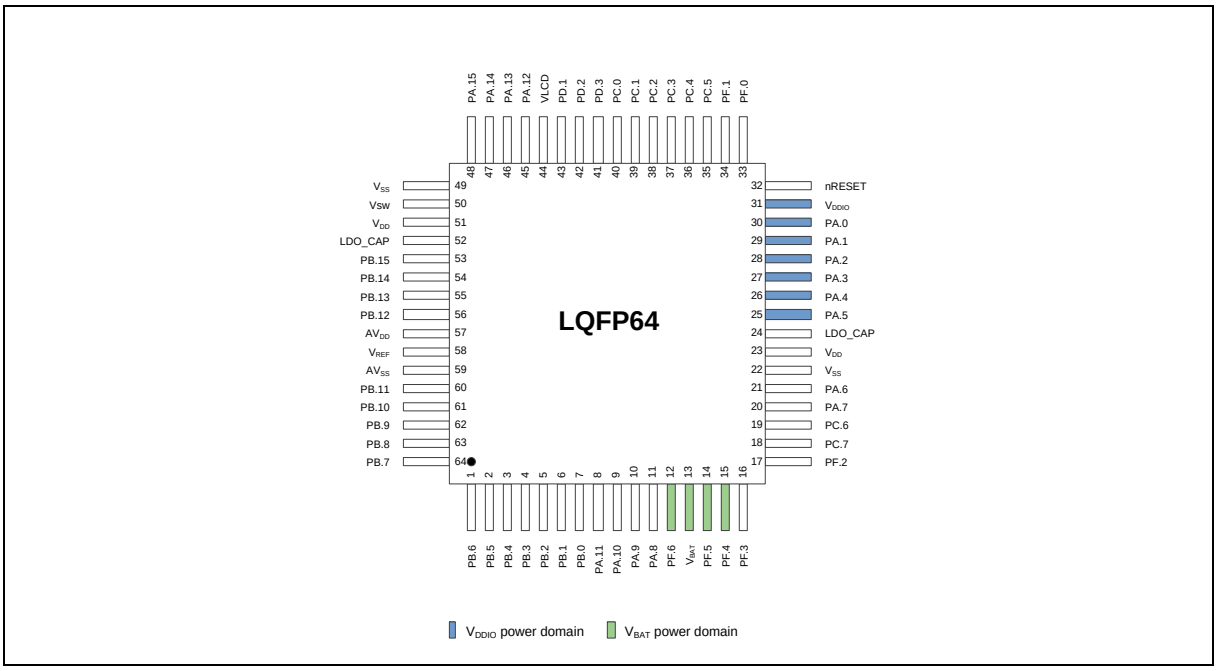


Figure 4.1-2 M2354 LQFP 64-pin Diagram

4.1.1.3 M2354 LQFP 128-Pin Diagram

Corresponding Part Number: M2354KJFAE

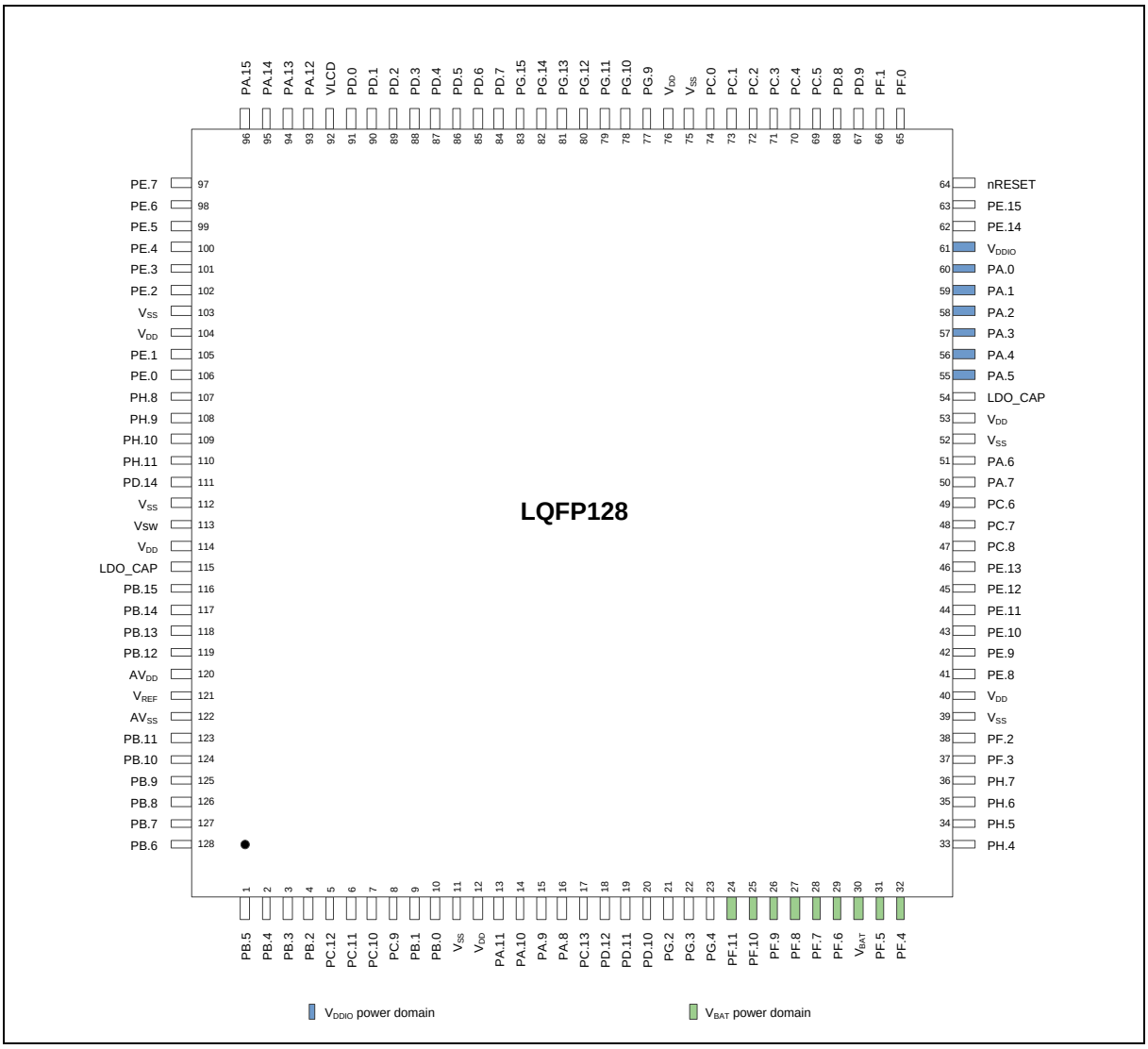


Figure 4.1-3 M2354 LQFP 128-pin Diagram

4.1.2 M2354 Multi-Function Pin Diagram

4.1.2.1 M2354 LQFP 48-Pin Multi-function Pin Diagram

Corresponding Part Number: M2354LJFAE

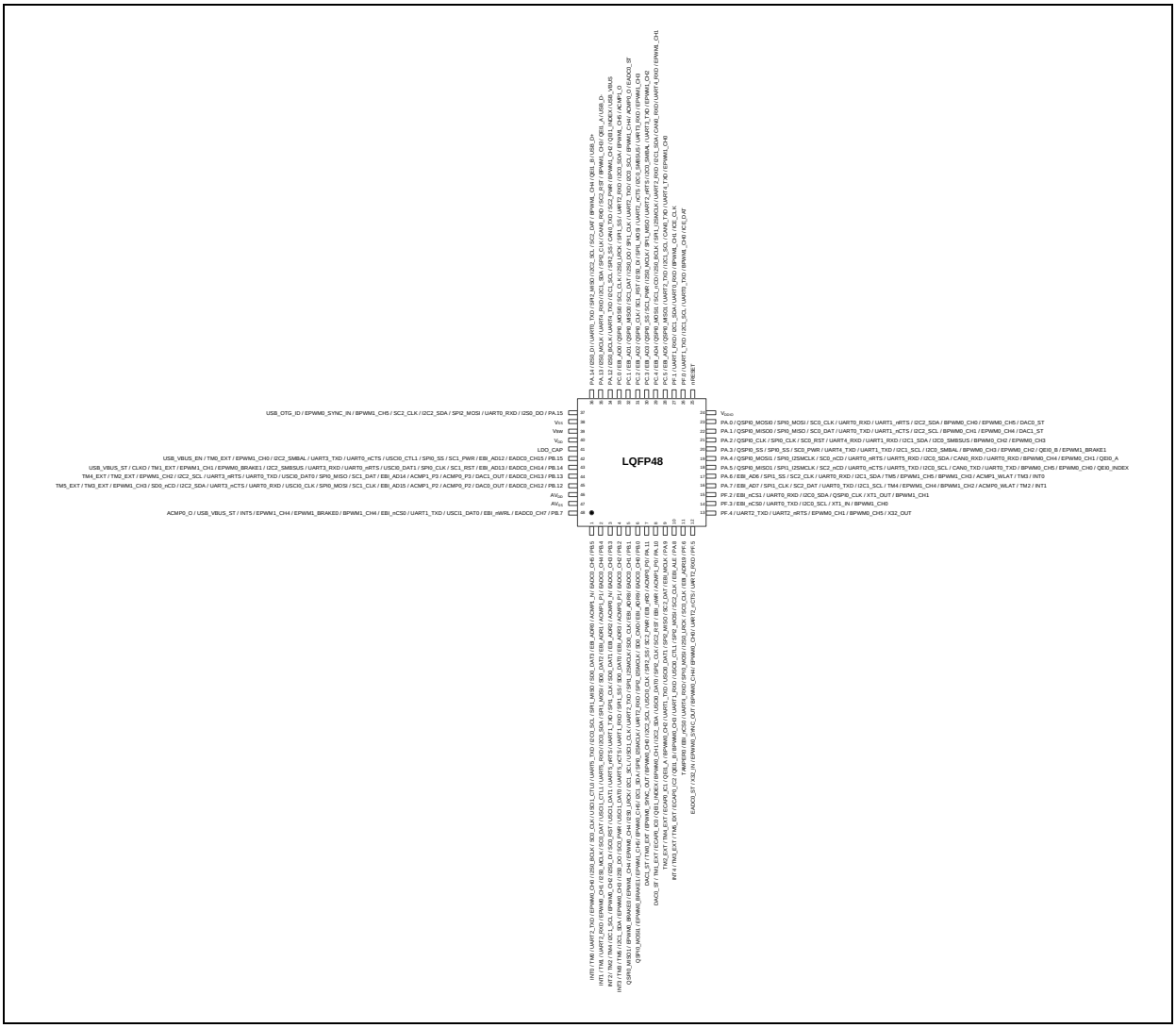


Figure 4.1-4 M2354LJFAE Multi-function Pin Diagram

Pin	M2354LJFAE Pin Function
1	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0
2	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1
3	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM4 / TM2 / INT2
4	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM5 / TM3 / INT3

Pin	M2354LJFAE Pin Function
5	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1
7	PA.11 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST
8	PA.10 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / QEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST
9	PA.9 / EBI_MCLK / SC2_DAT / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / QEI1_A / ECAP0_IC1 / TM4_EXT / TM2_EXT
10	PA.8 / EBI_ALE / SC2_CLK / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / QEI1_B / ECAP0_IC2 / TM5_EXT / TM3_EXT / INT4
11	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / TAMPER0
12	PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
13	PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
14	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
15	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
16	PA.7 / EBI_AD7 / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / TM4 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
17	PA.6 / EBI_AD6 / SPI1_SS / SC2_CLK / UART0_RXD / I2C1_SDA / TM5 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
18	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / QEI0_INDEX
19	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / QEI0_A
20	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / QEI0_B / EPWM1_BRAKE1
21	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3
22	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / DAC1_ST
23	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / DAC0_ST
24	V_{DDIO}
25	nRESET
26	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
27	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
28	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0
29	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1
30	PC.3 / EBI_AD3 / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD /

Pin	M2354LJFAE Pin Function
	EPWM1_CH2
31	PC.2 / EBI_AD2 / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3
32	PC.1 / EBI_AD1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ACMP0_O / EADC0_ST
33	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ACMP1_O
34	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / BPWM1_CH2 / QEI1_INDEX / USB_VBUS
35	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / BPWM1_CH3 / QEI1_A / USB_D-
36	PA.14 / I2S0_DI / UART0_TXD / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / QEI1_B / USB_D+
37	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID
38	V_{SS}
39	Vsw
40	V_{DD}
41	LDO_CAP
42	PB.15 / EADC0_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN
43	PB.14 / EADC0_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM0_BRAKE1 / EPWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
44	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / TM4_EXT
45	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / TM5_EXT
46	AV_{DD}
47	AV_{SS}
48	PB.7 / EADC0_CH7 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

Table 4.1-1 M2354LJFAE Multi-function Pin Table

4.1.2.2 M2354 LQFP 64-Pin Multi-function Pin Diagram

Corresponding Part Number: M2354SJFAE

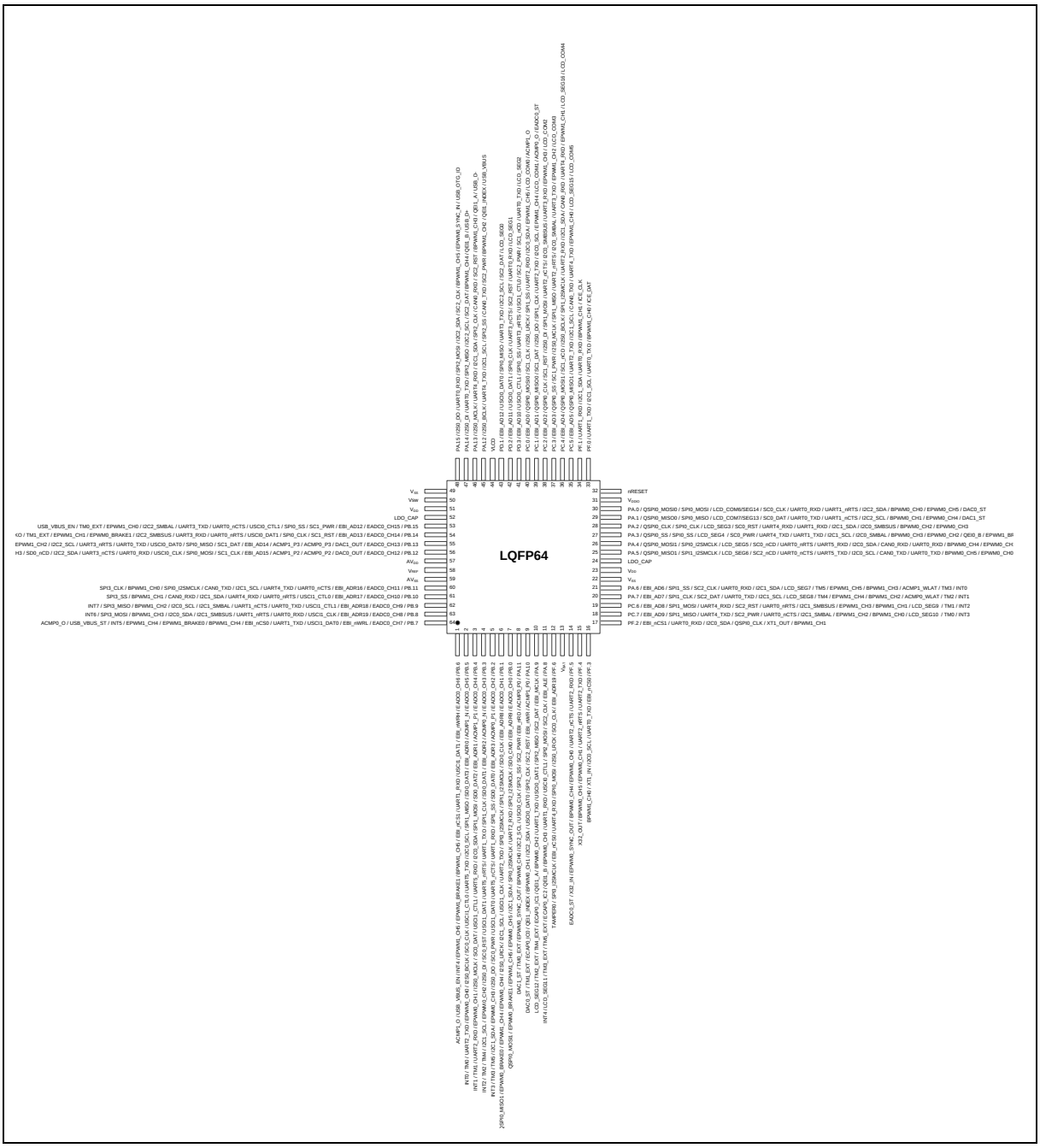


Figure 4.1-5 M2354SJFAE Multi-function Pin Diagram

Pin	M2354SJFAE Pin Function
1	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
2	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0

Pin	M2354SJFAE Pin Function
3	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1
4	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM4 / TM2 / INT2
5	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM5 / TM3 / INT3
6	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
7	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1
8	PA.11 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST
9	PA.10 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / QEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST
10	PA.9 / EBI_MCLK / SC2_DAT / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / QEI1_A / ECAP0_IC1 / TM4_EXT / TM2_EXT / LCD_SEG12
11	PA.8 / EBI_ALE / SC2_CLK / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / QEI1_B / ECAP0_IC2 / TM5_EXT / TM3_EXT / LCD_SEG11 / INT4
12	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / SPI3_I2SMCLK / TAMPER0
13	V_{BAT}
14	PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
15	PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
16	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
17	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
18	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / LCD_SEG10 / TM0 / INT3
19	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / LCD_SEG9 / TM1 / INT2
20	PA.7 / EBI_AD7 / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / LCD_SEG8 / TM4 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	PA.6 / EBI_AD6 / SPI1_SS / SC2_CLK / UART0_RXD / I2C1_SDA / LCD_SEG7 / TM5 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	V_{SS}
23	V_{DD}
24	LDO_CAP
25	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / LCD_SEG6 / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / QEI0_INDEX
26	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / LCD_SEG5 / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / QEI0_A
27	PA.3 / QSPI0_SS / SPI0_SS / LCD_SEG4 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / QEI0_B / EPWM1_BRAKE1

Pin	M2354SJFAE Pin Function
28	PA.2 / QSPI0_CLK / SPI0_CLK / LCD_SEG3 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3
29	PA.1 / QSPI0_MISO0 / SPI0_MISO / LCD_COM7/SEG13 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / DAC1_ST
30	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / LCD_COM6/SEG14 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / DAC0_ST
31	V_{DDIO}
32	nRESET
33	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
34	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
35	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / LCD_SEG15 / LCD_COM5
36	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / LCD_SEG16 / LCD_COM4
37	PC.3 / EBI_AD3 / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LCD_COM3
38	PC.2 / EBI_AD2 / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LCD_COM2
39	PC.1 / EBI_AD1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / LCD_COM1 / ACMP0_O / EADC0_ST
40	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / LCD_COM0 / ACMP1_O
41	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / SC2_PWR / SC1_nCD / UART0_TXD / LCD_SEG2
42	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / SC2_RST / UART0_RXD / LCD_SEG1
43	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL / SC2_DAT / LCD_SEG0
44	V_{LCD}
45	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / BPWM1_CH2 / QEI1_INDEX / USB_VBUS
46	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / BPWM1_CH3 / QEI1_A / USB_D-
47	PA.14 / I2S0_DI / UART0_TXD / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / QEI1_B / USB_D+
48	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID
49	V_{SS}
50	Vsw
51	V_{DD}
52	LDO_CAP
53	PB.15 / EADC0_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN

Pin	M2354SJFAE Pin Function
54	PB.14 / EADC0_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM0_BRAKE1 / EPWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
55	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / TM4_EXT
56	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / TM5_EXT
57	AV_{DD}
58	V_{REF}
59	AV_{SS}
60	PB.11 / EADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK
61	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS
62	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7
63	PB.8 / EADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6
64	PB.7 / EADC0_CH7 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

4.1.2.3 M2354 LQFP 128-Pin Multi-function Pin Diagram

Corresponding Part Number: M2354KJFAE

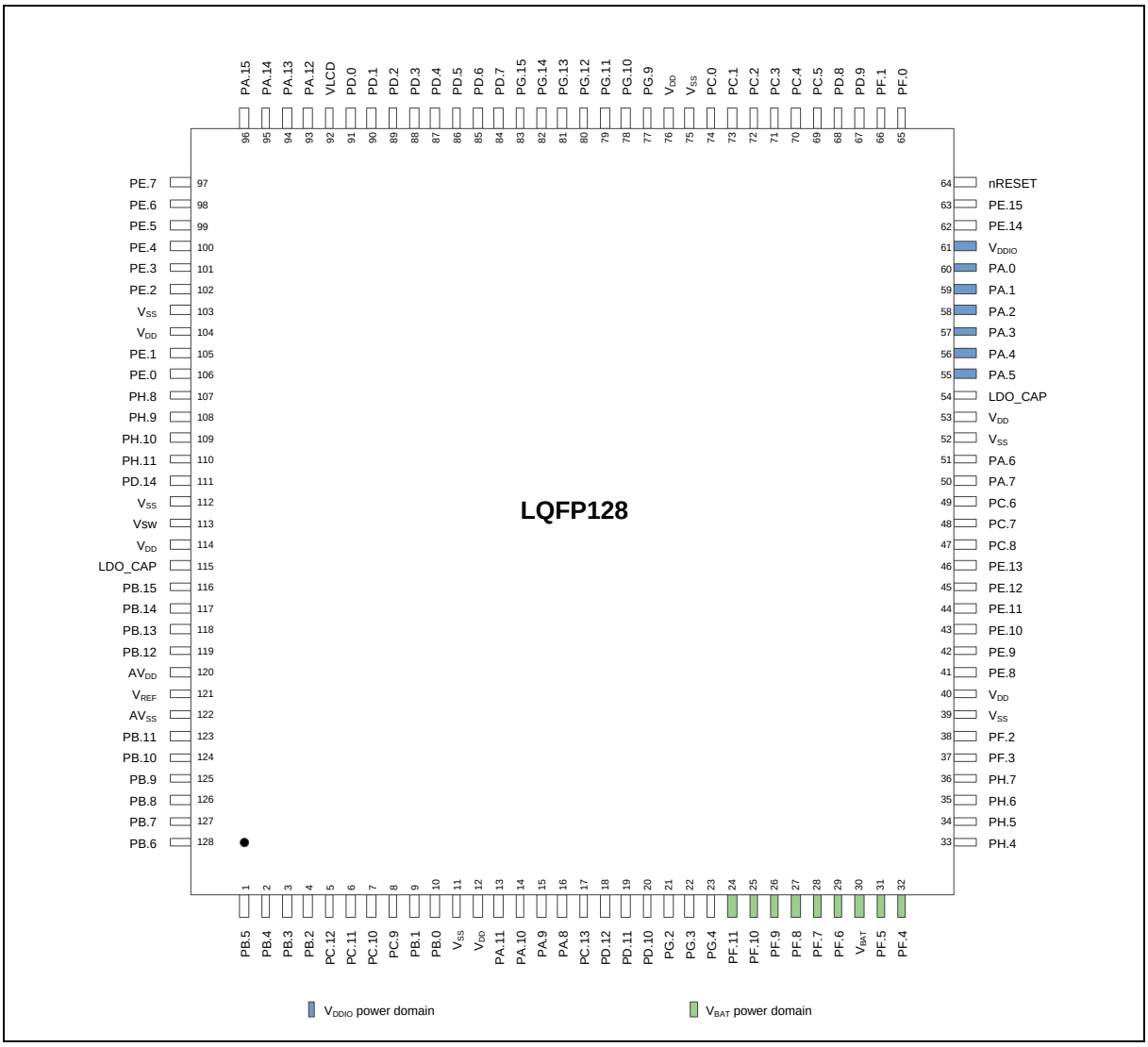


Figure 4.1-6 M2354KJFAE Multi-function Pin Diagram

Pin	M2354KJFAE Pin Function
1	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0
2	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1
3	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM4 / TM2 / INT2
4	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM5 / TM3 / INT3
5	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / SPI3_MISO / SC0_nCD / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O

Pin	M2354KJFAE Pin Function
6	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / SPI3_MOSI / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O
7	PC.10 / EBI_ADR6 / SPI3_CLK / UART3_TXD / ECAP1_IC0 / EPWM1_CH2
8	PC.9 / EBI_ADR7 / SPI3_SS / UART3_RXD / EPWM1_CH3
9	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
10	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1
11	V_{SS}
12	V_{DD}
13	PA.11 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST
14	PA.10 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / QEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST
15	PA.9 / EBI_MCLK / SC2_DAT / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / QEI1_A / ECAP0_IC1 / TM4_EXT / TM2_EXT
16	PA.8 / EBI_ALE / SC2_CLK / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / QEI1_B / ECAP0_IC2 / TM5_EXT / TM3_EXT / INT4
17	PC.13 / EBI_ADR10 / SC2_nCD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_TXD / BPWM0_CH4 / CLKO / EADC0_ST
18	PD.12 / EBI_nCS0 / UART2_RXD / BPWM0_CH5 / QEI0_INDEX / CLKO / EADC0_ST / INT5
19	PD.11 / EBI_nCS1 / UART1_TXD / CAN0_TXD / QEI0_A / INT6
20	PD.10 / EBI_nCS2 / UART1_RXD / CAN0_RXD / QEI0_B / INT7
21	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / TM0 / LCD_SEG39
22	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / TM1 / LCD_SEG38
23	PG.4 / EBI_ADR13 / SPI2_MISO / TM4 / TM2 / LCD_SEG37
24	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / TAMPER5 / TM5 / TM3
25	PF.10 / EBI_ADR15 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / TAMPER4
26	PF.9 / EBI_ADR16 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / TAMPER3
27	PF.8 / EBI_ADR17 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / TAMPER2
28	PF.7 / EBI_ADR18 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / TAMPER1
29	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / SPI3_I2SMCLK / TAMPER0
30	V_{BAT}
31	PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
32	PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
33	PH.4 / EBI_ADR3 / SPI1_MISO / LCD_SEG36
34	PH.5 / EBI_ADR2 / SPI1_MOSI / LCD_SEG35
35	PH.6 / EBI_ADR1 / SPI1_CLK / LCD_SEG34

Pin	M2354KJFAE Pin Function
36	PH.7 / EBI_ADR0 / SPI1_SS / LCD_SEG33
37	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
38	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
39	V_{SS}
40	V_{DD}
41	PE.8 / EBI_ADR10 / I2S0_BCLK / SPI2_CLK / USCI1_CTL1 / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / TRACE_DATA3 / LCD_SEG32
42	PE.9 / EBI_ADR11 / I2S0_MCLK / SPI2_MISO / USCI1_CTL0 / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / TRACE_DATA2 / LCD_SEG31
43	PE.10 / EBI_ADR12 / I2S0_DI / SPI2_MOSI / USCI1_DAT0 / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / TRACE_DATA1 / LCD_SEG30
44	PE.11 / EBI_ADR13 / I2S0_DO / SPI2_SS / USCI1_DAT1 / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0
45	PE.12 / EBI_ADR14 / I2S0_LRCK / SPI2_I2SMCLK / USCI1_CLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK
46	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0
47	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4
48	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3
49	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2
50	PA.7 / EBI_AD7 / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / TM4 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
51	PA.6 / EBI_AD6 / SPI1_SS / SC2_CLK / UART0_RXD / I2C1_SDA / TM5 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	V_{SS}
53	V_{DD}
54	LDO_CAP
55	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / QEI0_INDEX / LCD_SEG29
56	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / QEI0_A / LCD_SEG28
57	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / LCD_SEG27 / BPWM0_CH3 / EPWM0_CH2 / QEI0_B / EPWM1_BRAKE1
58	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / LCD_SEG26 / BPWM0_CH2 / EPWM0_CH3
59	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / LCD_SEG25 / BPWM0_CH1 / EPWM0_CH4 / DAC1_ST
60	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / LCD_SEG24 / BPWM0_CH0 / EPWM0_CH5 / DAC0_ST

Pin	M2354KJFAE Pin Function
61	V_{DDIO}
62	PE.14 / EBI_AD8 / UART2_TXD / CAN0_TXD / LCD_SEG23
63	PE.15 / EBI_AD9 / UART2_RXD / CAN0_RXD / LCD_SEG22
64	nRESET
65	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
66	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
67	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / LCD_COM7/SEG40
68	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / LCD_COM6/SEG41
69	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / LCD_COM5/SEG42
70	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / LCD_COM4/SEG43
71	PC.3 / EBI_AD3 / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LCD_COM3
72	PC.2 / EBI_AD2 / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LCD_COM2
73	PC.1 / EBI_AD1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / LCD_COM1 / ACMP0_O / EADC0_ST
74	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / LCD_COM0 / ACMP1_O
75	V_{SS}
76	V_{DD}
77	PG.9 / EBI_AD0 / BPWM0_CH5 / LCD_SEG21
78	PG.10 / EBI_AD1 / BPWM0_CH4 / LCD_SEG20
79	PG.11 / EBI_AD2 / BPWM0_CH3 / LCD_SEG19
80	PG.12 / EBI_AD3 / BPWM0_CH2 / LCD_SEG18
81	PG.13 / EBI_AD4 / BPWM0_CH1 / LCD_SEG17
82	PG.14 / EBI_AD5 / BPWM0_CH0 / LCD_SEG16
83	PG.15 / LCD_SEG15 / CLKO / EADC0_ST
84	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK / SC1_PWR / LCD_SEG14
85	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1 / SC1_RST / LCD_SEG13
86	PD.5 / I2C1_SCL / SPI1_CLK / USCI1_DAT0 / SC1_DAT
87	PD.4 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / SC1_CLK / USB_VBUS_ST
88	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / SC2_PWR / SC1_nCD / UART0_TXD
89	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / SC2_RST / UART0_RXD
90	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL / SC2_DAT

Pin	M2354KJFAE Pin Function
91	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / SC2_CLK / TM2
92	V_{LCD}
93	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / BPWM1_CH2 / QEI1_INDEX / USB_VBUS
94	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / BPWM1_CH3 / QEI1_A / USB_D-
95	PA.14 / I2S0_DI / UART0_TXD / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / QEI1_B / USB_D+
96	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID
97	PE.7 / SD0_CMD / UART5_TXD / QEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / LCD_SEG12
98	PE.6 / SD0_CLK / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / QEI1_A / EPWM0_CH1 / BPWM0_CH4 / LCD_SEG11
99	PE.5 / EBI_nRD / SD0_DAT3 / SPI3_SS / SC0_PWR / USCI0_CTL1 / QEI1_B / EPWM0_CH2 / BPWM0_CH3 / LCD_SEG10
100	PE.4 / EBI_nWR / SD0_DAT2 / SPI3_CLK / SC0_RST / USCI0_DAT1 / QEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / LCD_SEG9
101	PE.3 / EBI_MCLK / SD0_DAT1 / SPI3_MISO / SC0_DAT / USCI0_DAT0 / QEI0_A / EPWM0_CH4 / BPWM0_CH1 / LCD_SEG8
102	PE.2 / EBI_ALE / SD0_DAT0 / SPI3_MOSI / SC0_CLK / USCI0_CLK / QEI0_B / EPWM0_CH5 / BPWM0_CH0 / LCD_SEG7
103	V_{SS}
104	V_{DD}
105	PE.1 / EBI_AD10 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / LCD_SEG6
106	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / LCD_SEG5
107	PH.8 / EBI_AD12 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / LCD_SEG4
108	PH.9 / EBI_AD13 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / LCD_SEG3
109	PH.10 / EBI_AD14 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / LCD_SEG2
110	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / LCD_SEG1
111	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SC1_nCD / USCI0_CTL0 / SPI0_I2SMCLK / EPWM0_CH4 / LCD_SEG0
112	V_{SS}
113	Vsw
114	V_{DD}
115	LDO_CAP
116	PB.15 / EADC0_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN

Pin	M2354KJFAE Pin Function
117	PB.14 / EADC0_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM0_BRAKE1 / EPWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
118	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / TM4_EXT
119	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / TM5_EXT
120	AV_{DD}
121	V_{REF}
122	AV_{SS}
123	PB.11 / EADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK
124	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS
125	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7
126	PB.8 / EADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6
127	PB.7 / EADC0_CH7 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
128	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.1-2 M2354KJFAE Multi-function Pin Table

4.2 M2354 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfigure.

Corresponding Part Number: M2354

	M2354		
Pin Name	48 Pin	64 Pin	128 Pin
PB.6		1	128
PB.5	1	2	1
PB.4	2	3	2
PB.3	3	4	3
PB.2	4	5	4
PC.12			5
PC.11			6
PC.10			7
PC.9			8
PB.1	5	6	9
PB.0	6	7	10
V_{SS}			11
V_{DD}			12
PA.11	7	8	13
PA.10	8	9	14
PA.9	9	10	15
PA.8	10	11	16
PC.13			17
PD.12			18
PD.11			19
PD.10			20
PG.2			21
PG.3			22
PG.4			23
PF.11			24
PF.10			25
PF.9			26
PF.8			27
PF.7			28

PF.6	11	12	29
V_{BAT}		13	30
PF.5	12	14	31
PF.4	13	15	32
PH.4			33
PH.5			34
PH.6			35
PH.7			36
PF.3	14	16	37
PF.2	15	17	38
V_{SS}			39
V_{DD}			40
PE.8			41
PE.9			42
PE.10			43
PE.11			44
PE.12			45
PE.13			46
PC.8			47
PC.7		18	48
PC.6		19	49
PA.7	16	20	50
PA.6	17	21	51
V_{SS}		22	52
V_{DD}		23	53
LDO_CAP		24	54
PA.5	18	25	55
PA.4	19	26	56
PA.3	20	27	57
PA.2	21	28	58
PA.1	22	29	59
PA.0	23	30	60
V_{DDIO}	24	31	61
PE.14			62

PE.15			63
nRESET	25	32	64
PF.0	26	33	65
PF.1	27	34	66
PD.9			67
PD.8			68
PC.5	28	35	69
PC.4	29	36	70
PC.3	30	37	71
PC.2	31	38	72
PC.1	32	39	73
PC.0	33	40	74
V_{SS}			75
V_{DD}			76
PG.9			77
PG.10			78
PG.11			79
PG.12			80
PG.13			81
PG.14			82
PG.15			83
PD.7			84
PD.6			85
PD.5			86
PD.4			87
PD.3		41	88
PD.2		42	89
PD.1		43	90
PD.0			91
V_{LCD}		44	92
PA.12	34	45	93
PA.13	35	46	94
PA.14	36	47	95
PA.15	37	48	96

PE.7			97
PE.6			98
PE.5			99
PE.4			100
PE.3			101
PE.2			102
V_{SS}	38	49	103
V_{DD}			104
PE.1			105
PE.0			106
PH.8			107
PH.9			108
PH.10			109
PH.11			110
PD.14			111
V_{SS}			112
V_{sw}	39	50	113
V_{DD}	40	51	114
LDO_CAP	41	52	115
PB.15	42	53	116
PB.14	43	54	117
PB.13	44	55	118
PB.12	45	56	119
AV_{DD}	46	57	120
V_{REF}		58	121
AV_{SS}	47	59	122
PB.11		60	123
PB.10		61	124
PB.9		62	125
PB.8		63	126
PB.7	48	64	127

4.3 M2354 Pin Functional Description

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N	PB.3	MFP1	A	Analog comparator 0 negative input pin.
	ACMP0_O	PC.12	MFP14	O	Analog comparator 0 output pin.
		PC.1	MFP14	O	
		PB.7	MFP15	O	
	ACMP0_P0	PA.11	MFP1	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.2	MFP1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.12	MFP1	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.13	MFP1	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PA.7	MFP13	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PB.5	MFP1	A	Analog comparator 1 negative input pin.
	ACMP1_O	PB.6	MFP15	O	Analog comparator 1 output pin.
		PC.11	MFP14	O	
		PC.0	MFP14	O	
	ACMP1_P0	PA.10	MFP1	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PB.4	MFP1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PB.12	MFP1	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PB.13	MFP1	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PA.6	MFP13	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	PA.11	MFP9	I/O	BPWM0 channel 0 output/capture input.
		PA.0	MFP12	I/O	
		PG.14	MFP12	I/O	
		PE.2	MFP13	I/O	
	BPWM0_CH1	PA.10	MFP9	I/O	BPWM0 channel 1 output/capture input.
		PA.1	MFP12	I/O	
		PG.13	MFP12	I/O	
		PE.3	MFP13	I/O	
	BPWM0_CH2	PA.9	MFP9	I/O	BPWM0 channel 2 output/capture input.
		PA.2	MFP12	I/O	
		PG.12	MFP12	I/O	
		PE.4	MFP13	I/O	
	BPWM0_CH3	PA.8	MFP9	I/O	BPWM0 channel 3 output/capture input.
		PA.3	MFP12	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PG.11	MFP12	I/O	
		PE.5	MFP13	I/O	
	BPWM0_CH4	PC.13	MFP9	I/O	BPWM0 channel 4 output/capture input.
		PF.5	MFP8	I/O	
		PA.4	MFP12	I/O	
		PG.10	MFP12	I/O	
		PE.6	MFP13	I/O	
	BPWM0_CH5	PD.12	MFP9	I/O	BPWM0 channel 5 output/capture input.
		PF.4	MFP8	I/O	
		PA.5	MFP12	I/O	
		PG.9	MFP12	I/O	
		PE.7	MFP13	I/O	
BPWM1	BPWM1_CH0	PF.3	MFP11	I/O	BPWM1 channel 0 output/capture input.
		PC.7	MFP12	I/O	
		PF.0	MFP12	I/O	
		PB.11	MFP10	I/O	
	BPWM1_CH1	PF.2	MFP11	I/O	BPWM1 channel 1 output/capture input.
		PC.6	MFP12	I/O	
		PF.1	MFP12	I/O	
		PB.10	MFP10	I/O	
	BPWM1_CH2	PA.7	MFP12	I/O	BPWM1 channel 2 output/capture input.
		PA.12	MFP11	I/O	
		PB.9	MFP10	I/O	
	BPWM1_CH3	PA.6	MFP12	I/O	BPWM1 channel 3 output/capture input.
		PA.13	MFP11	I/O	
		PB.8	MFP10	I/O	
	BPWM1_CH4	PC.8	MFP12	I/O	BPWM1 channel 4 output/capture input.
		PA.14	MFP11	I/O	
		PB.7	MFP10	I/O	
	BPWM1_CH5	PB.6	MFP10	I/O	BPWM1 channel 5 output/capture input.
		PE.13	MFP12	I/O	
		PA.15	MFP11	I/O	
CAN0	CAN0_RXD	PD.10	MFP4	I	CAN0 bus receiver input.

Group	Pin Name	GPIO	MFP	Type	Description
		PA.4	MFP10	I	
		PE.15	MFP4	I	
		PC.4	MFP10	I	
		PA.13	MFP6	I	
		PB.10	MFP8	I	
	CAN0_TXD	PD.11	MFP4	O	CAN0 bus transmitter output.
		PA.5	MFP10	O	
		PE.14	MFP4	O	
		PC.5	MFP10	O	
		PA.12	MFP6	O	
		PB.11	MFP8	O	
CLKO	CLKO	PC.13	MFP13	O	Clock Out
		PD.12	MFP13	O	
		PG.15	MFP14	O	
		PB.14	MFP14	O	
DAC0	DAC0_OUT	PB.12	MFP1	A	DAC0 channel analog output.
		PB.12	MFP1	A	
	DAC0_ST	PA.10	MFP14	I	DAC0 external trigger input.
		PA.0	MFP15	I	
DAC1	DAC1_OUT	PB.13	MFP1	A	DAC1 channel analog output.
		PB.13	MFP1	A	
	DAC1_ST	PA.11	MFP14	I	DAC1 external trigger input.
		PA.1	MFP15	I	
EADC0	EADC0_CH0	PB.0	MFP1	A	EADC0 channel 0 analog input.
	EADC0_CH1	PB.1	MFP1	A	EADC0 channel 1 analog input.
	EADC0_CH2	PB.2	MFP1	A	EADC0 channel 2 analog input.
	EADC0_CH3	PB.3	MFP1	A	EADC0 channel 3 analog input.
	EADC0_CH4	PB.4	MFP1	A	EADC0 channel 4 analog input.
	EADC0_CH5	PB.5	MFP1	A	EADC0 channel 5 analog input.
	EADC0_CH6	PB.6	MFP1	A	EADC0 channel 6 analog input.
	EADC0_CH7	PB.7	MFP1	A	EADC0 channel 7 analog input.
	EADC0_CH8	PB.8	MFP1	A	EADC0 channel 8 analog input.
	EADC0_CH9	PB.9	MFP1	A	EADC0 channel 9 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	EADC0_CH10	PB.10	MFP1	A	EADC0 channel 10 analog input.
	EADC0_CH11	PB.11	MFP1	A	EADC0 channel 11 analog input.
	EADC0_CH12	PB.12	MFP1	A	EADC0 channel 12 analog input.
	EADC0_CH13	PB.13	MFP1	A	EADC0 channel 13 analog input.
	EADC0_CH14	PB.14	MFP1	A	EADC0 channel 14 analog input.
	EADC0_CH15	PB.15	MFP1	A	EADC0 channel 15 analog input.
	EADC0_ST	PC.13	MFP14	I	EADC0 external trigger input.
		PD.12	MFP14	I	
		PF.5	MFP11	I	
		PC.1	MFP15	I	
		PG.15	MFP15	I	
EBI	EBI_AD0	PC.0	MFP2	I/O	EBI address/data bus bit 0.
		PG.9	MFP2	I/O	
	EBI_AD1	PC.1	MFP2	I/O	EBI address/data bus bit 1.
		PG.10	MFP2	I/O	
	EBI_AD2	PC.2	MFP2	I/O	EBI address/data bus bit 2.
		PG.11	MFP2	I/O	
	EBI_AD3	PC.3	MFP2	I/O	EBI address/data bus bit 3.
		PG.12	MFP2	I/O	
	EBI_AD4	PC.4	MFP2	I/O	EBI address/data bus bit 4.
		PG.13	MFP2	I/O	
	EBI_AD5	PC.5	MFP2	I/O	EBI address/data bus bit 5.
		PG.14	MFP2	I/O	
	EBI_AD6	PA.6	MFP2	I/O	EBI address/data bus bit 6.
		PD.8	MFP2	I/O	
	EBI_AD7	PA.7	MFP2	I/O	EBI address/data bus bit 7.
		PD.9	MFP2	I/O	
	EBI_AD8	PC.6	MFP2	I/O	EBI address/data bus bit 8.
		PE.14	MFP2	I/O	
	EBI_AD9	PC.7	MFP2	I/O	EBI address/data bus bit 9.
		PE.15	MFP2	I/O	
	EBI_AD10	PD.3	MFP2	I/O	EBI address/data bus bit 10.
		PE.1	MFP2	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_AD11	PD.2	MFP2	I/O	EBI address/data bus bit 11.
		PE.0	MFP2	I/O	
	EBI_AD12	PD.1	MFP2	I/O	EBI address/data bus bit 12.
		PH.8	MFP2	I/O	
		PB.15	MFP2	I/O	
	EBI_AD13	PD.0	MFP2	I/O	EBI address/data bus bit 13.
		PH.9	MFP2	I/O	
		PB.14	MFP2	I/O	
	EBI_AD14	PH.10	MFP2	I/O	EBI address/data bus bit 14.
		PB.13	MFP2	I/O	
	EBI_AD15	PH.11	MFP2	I/O	EBI address/data bus bit 15.
		PB.12	MFP2	I/O	
	EBI_ADR0	PB.5	MFP2	O	EBI address bus bit 0.
		PH.7	MFP2	O	
	EBI_ADR1	PB.4	MFP2	O	EBI address bus bit 1.
		PH.6	MFP2	O	
	EBI_ADR2	PB.3	MFP2	O	EBI address bus bit 2.
		PH.5	MFP2	O	
	EBI_ADR3	PB.2	MFP2	O	EBI address bus bit 3.
		PH.4	MFP2	O	
	EBI_ADR4	PC.12	MFP2	O	EBI address bus bit 4.
	EBI_ADR5	PC.11	MFP2	O	EBI address bus bit 5.
	EBI_ADR6	PC.10	MFP2	O	EBI address bus bit 6.
	EBI_ADR7	PC.9	MFP2	O	EBI address bus bit 7.
	EBI_ADR8	PB.1	MFP2	O	EBI address bus bit 8.
	EBI_ADR9	PB.0	MFP2	O	EBI address bus bit 9.
	EBI_ADR10	PC.13	MFP2	O	EBI address bus bit 10.
		PE.8	MFP2	O	
	EBI_ADR11	PG.2	MFP2	O	EBI address bus bit 11.
		PE.9	MFP2	O	
	EBI_ADR12	PG.3	MFP2	O	EBI address bus bit 12.
		PE.10	MFP2	O	
	EBI_ADR13	PG.4	MFP2	O	EBI address bus bit 13.

Group	Pin Name	GPIO	MFP	Type	Description
		PE.11	MFP2	O	
	EBI_ADR14	PF.11	MFP2	O	EBI address bus bit 14.
		PE.12	MFP2	O	
	EBI_ADR15	PF.10	MFP2	O	EBI address bus bit 15.
		PE.13	MFP2	O	
	EBI_ADR16	PF.9	MFP2	O	EBI address bus bit 16.
		PC.8	MFP2	O	
		PB.11	MFP2	O	
	EBI_ADR17	PF.8	MFP2	O	EBI address bus bit 17.
		PB.10	MFP2	O	
	EBI_ADR18	PF.7	MFP2	O	EBI address bus bit 18.
		PB.9	MFP2	O	
	EBI_ADR19	PF.6	MFP2	O	EBI address bus bit 19.
		PB.8	MFP2	O	
	EBI_ALE	PA.8	MFP2	O	EBI address latch enable output pin.
		PE.2	MFP2	O	
	EBI_MCLK	PA.9	MFP2	O	EBI external clock output pin.
		PE.3	MFP2	O	
	EBI_nCS0	PD.12	MFP2	O	EBI chip select 0 output pin.
		PF.6	MFP7	O	
		PF.3	MFP2	O	
		PD.14	MFP2	O	
		PB.7	MFP8	O	
	EBI_nCS1	PB.6	MFP8	O	EBI chip select 1 output pin.
		PD.11	MFP2	O	
		PF.2	MFP2	O	
	EBI_nCS2	PD.10	MFP2	O	EBI chip select 2 output pin.
	EBI_nRD	PA.11	MFP2	O	EBI read enable output pin.
		PE.5	MFP2	O	
	EBI_nWR	PA.10	MFP2	O	EBI write enable output pin.
		PE.4	MFP2	O	
	EBI_nWRH	PB.6	MFP2	O	EBI high byte write enable output pin
	EBI_nWRL	PB.7	MFP2	O	EBI low byte write enable output pin.

Group	Pin Name	GPIO	MFP	Type	Description
ECAP0	ECAP0_IC0	PA.10	MFP11	I	Enhanced capture unit 0 input 0 pin.
		PE.8	MFP12	I	
	ECAP0_IC1	PA.9	MFP11	I	Enhanced capture unit 0 input 1 pin.
		PE.9	MFP12	I	
	ECAP0_IC2	PA.8	MFP11	I	Enhanced capture unit 0 input 2 pin.
		PE.10	MFP12	I	
ECAP1	ECAP1_IC0	PC.10	MFP11	I	Enhanced capture unit 1 input 0 pin.
		PE.13	MFP13	I	
	ECAP1_IC1	PC.11	MFP11	I	Enhanced capture unit 1 input 1 pin.
		PE.12	MFP13	I	
	ECAP1_IC2	PC.12	MFP11	I	Enhanced capture unit 1 input 2 pin.
		PE.11	MFP13	I	
EPWM0	EPWM0_BRAKE0	PB.1	MFP13	I	EPWM0 Brake 0 input pin.
		PE.8	MFP11	I	
	EPWM0_BRAKE1	PB.0	MFP13	I	EPWM0 Brake 1 input pin.
		PE.9	MFP11	I	
		PB.14	MFP10	I	
	EPWM0_CH0	PB.5	MFP11	I/O	EPWM0 channel 0 output/capture input.
		PF.5	MFP7	I/O	
		PE.8	MFP10	I/O	
		PA.5	MFP13	I/O	
		PE.7	MFP12	I/O	
	EPWM0_CH1	PB.4	MFP11	I/O	EPWM0 channel 1 output/capture input.
		PF.4	MFP7	I/O	
		PE.9	MFP10	I/O	
		PA.4	MFP13	I/O	
		PE.6	MFP12	I/O	
	EPWM0_CH2	PB.3	MFP11	I/O	EPWM0 channel 2 output/capture input.
		PE.10	MFP10	I/O	
		PA.3	MFP13	I/O	
		PE.5	MFP12	I/O	
	EPWM0_CH3	PB.2	MFP11	I/O	EPWM0 channel 3 output/capture input.
		PE.11	MFP10	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PA.2	MFP13	I/O	
		PE.4	MFP12	I/O	
	EPWM0_CH4	PB.1	MFP11	I/O	EPWM0 channel 4 output/capture input.
		PE.12	MFP10	I/O	
		PA.1	MFP13	I/O	
		PE.3	MFP12	I/O	
		PD.14	MFP11	I/O	
	EPWM0_CH5	PB.0	MFP11	I/O	EPWM0 channel 5 output/capture input.
		PE.13	MFP10	I/O	
		PA.0	MFP13	I/O	
		PE.2	MFP12	I/O	
		PH.11	MFP11	I/O	
	EPWM0_SYNC_IN	PA.15	MFP12	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	PA.11	MFP10	O	EPWM0 counter synchronous trigger output pin.
		PF.5	MFP9	O	
EPWM1	EPWM1_BRAKE0	PE.10	MFP11	I	EPWM1 Brake 0 input pin.
		PB.7	MFP11	I	
	EPWM1_BRAKE1	PB.6	MFP11	I	EPWM1 Brake 1 input pin.
		PE.11	MFP11	I	
		PA.3	MFP15	I	
	EPWM1_CH0	PC.12	MFP12	I/O	EPWM1 channel 0 output/capture input.
		PE.13	MFP11	I/O	
		PC.5	MFP12	I/O	
		PB.15	MFP11	I/O	
	EPWM1_CH1	PC.11	MFP12	I/O	EPWM1 channel 1 output/capture input.
		PC.8	MFP11	I/O	
		PC.4	MFP12	I/O	
		PB.14	MFP11	I/O	
	EPWM1_CH2	PC.10	MFP12	I/O	EPWM1 channel 2 output/capture input.
		PC.7	MFP11	I/O	
		PC.3	MFP12	I/O	
		PB.13	MFP11	I/O	
	EPWM1_CH3	PC.9	MFP12	I/O	EPWM1 channel 3 output/capture input.

Group	Pin Name	GPIO	MFP	Type	Description
		PC.6	MFP11	I/O	
		PC.2	MFP12	I/O	
		PB.12	MFP11	I/O	
	EPWM1_CH4	PB.1	MFP12	I/O	EPWM1 channel 4 output/capture input.
		PA.7	MFP11	I/O	
		PC.1	MFP12	I/O	
		PB.7	MFP12	I/O	
	EPWM1_CH5	PB.6	MFP12	I/O	EPWM1 channel 5 output/capture input.
		PB.0	MFP12	I/O	
		PA.6	MFP11	I/O	
		PC.0	MFP12	I/O	
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I2C0 clock pin.
		PC.12	MFP4	I/O	
		PF.3	MFP4	I/O	
		PE.13	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
		PD.7	MFP4	I/O	
		PB.9	MFP9	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I2C0 data input/output pin.
		PC.11	MFP4	I/O	
		PF.2	MFP4	I/O	
		PC.8	MFP4	I/O	
		PA.4	MFP9	I/O	
		PC.0	MFP9	I/O	
		PD.6	MFP4	I/O	
		PB.8	MFP9	I/O	
	I2C0_SMBAL	PG.2	MFP4	O	I2C0 SMBus SMBALTER pin
		PA.3	MFP10	O	
		PC.3	MFP9	O	
	I2C0_SMBSUS	PG.3	MFP4	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
		PA.2	MFP10	O	
		PC.2	MFP9	O	

Group	Pin Name	GPIO	MFP	Type	Description
I2C1	I2C1_SCL	PB.3	MFP12	I/O	I2C1 clock pin.
		PB.1	MFP9	I/O	
		PG.2	MFP5	I/O	
		PA.7	MFP8	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
		PD.5	MFP4	I/O	
		PA.12	MFP4	I/O	
		PE.1	MFP8	I/O	
		PB.11	MFP7	I/O	
	I2C1_SDA	PB.2	MFP12	I/O	I2C1 data input/output pin.
		PB.0	MFP9	I/O	
		PG.3	MFP5	I/O	
		PA.6	MFP8	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	
		PC.4	MFP9	I/O	
		PD.4	MFP4	I/O	
		PA.13	MFP4	I/O	
		PE.0	MFP8	I/O	
		PB.10	MFP7	I/O	
	I2C1_SMBAL	PC.7	MFP8	O	I2C1 SMBus SMBALTER pin
		PH.8	MFP8	O	
		PB.9	MFP7	O	
	I2C1_SMBSUS	PC.6	MFP8	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
		PH.9	MFP8	O	
		PB.8	MFP7	O	
I2C2	I2C2_SCL	PA.11	MFP7	I/O	I2C2 clock pin.
		PA.1	MFP9	I/O	
		PD.9	MFP3	I/O	
		PD.1	MFP6	I/O	
		PA.14	MFP6	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PH.8	MFP9	I/O	
		PB.13	MFP8	I/O	
	I2C2_SDA	PA.10	MFP7	I/O	I2C2 data input/output pin.
		PA.0	MFP9	I/O	
		PD.8	MFP3	I/O	
		PD.0	MFP6	I/O	
		PA.15	MFP6	I/O	
		PH.9	MFP9	I/O	
		PB.12	MFP8	I/O	
	I2C2_SMBAL	PB.15	MFP8	O	I2C2 SMBus SMBALTER pin
	I2C2_SMBSUS	PB.14	MFP8	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	PB.5	MFP10	O	I2S0 bit clock output pin.
		PF.10	MFP4	O	
		PE.8	MFP4	O	
		PC.4	MFP6	O	
		PA.12	MFP2	O	
		PE.1	MFP5	O	
	I2S0_DI	PB.3	MFP10	I	I2S0 data input pin.
		PF.8	MFP4	I	
		PE.10	MFP4	I	
		PC.2	MFP6	I	
		PA.14	MFP2	I	
		PH.8	MFP5	I	
	I2S0_DO	PB.2	MFP10	O	I2S0 data output pin.
		PF.7	MFP4	O	
		PE.11	MFP4	O	
		PC.1	MFP6	O	
		PA.15	MFP2	O	
		PH.9	MFP5	O	
	I2S0_LRCK	PB.1	MFP10	O	I2S0 left right channel clock output pin.
		PF.6	MFP4	O	
		PE.12	MFP4	O	
		PC.0	MFP6	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PH.10	MFP5	O	
	I2S0_MCLK	PB.4	MFP10	O	I2S0 master clock output pin.
		PF.9	MFP4	O	
		PE.9	MFP4	O	
		PC.3	MFP6	O	
		PA.13	MFP2	O	
		PE.0	MFP5	O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	PF.0	MFP14	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.
		PA.7	MFP15	I	
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
		PC.6	MFP15	I	
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
		PC.7	MFP15	I	
INT4	INT4	PB.6	MFP13	I	External interrupt 4 input pin.
		PA.8	MFP15	I	
INT5	INT5	PD.12	MFP15	I	External interrupt 5 input pin.
		PB.7	MFP13	I	
INT6	INT6	PD.11	MFP15	I	External interrupt 6 input pin.
		PB.8	MFP13	I	
INT7	INT7	PD.10	MFP15	I	External interrupt 7 input pin.
		PB.9	MFP13	I	
LCD	LCD_COM0	PC.0	MFP13	A	LCD common 0 output pin
	LCD_COM1	PC.1	MFP13	A	LCD common 1 output pin
	LCD_COM2	PC.2	MFP15	A	LCD common 2 output pin
	LCD_COM3	PC.3	MFP15	A	LCD common 3 output pin
	LCD_COM4/SEG43	PC.4	MFP15	A	LCD common 4 output pin
	LCD_COM5/SEG42	PC.5	MFP15	A	LCD common 5 output pin

Group	Pin Name	GPIO	MFP	Type	Description
	LCD_COM6/SEG41	PD.8	MFP15	A	LCD common 6 output pin
	LCD_COM7/SEG40	PD.9	MFP15	A	LCD common 7 output pin
	LCD_SEG0	PD.14	MFP15	A	LCD segment 0 output pin
	LCD_SEG1	PH.11	MFP15	A	LCD segment 1 output pin
	LCD_SEG2	PH.10	MFP15	A	LCD segment 2 output pin
	LCD_SEG3	PH.9	MFP15	A	LCD segment 3 output pin
	LCD_SEG4	PH.8	MFP15	A	LCD segment 4 output pin
	LCD_SEG5	PE.0	MFP15	A	LCD segment 5 output pin
	LCD_SEG6	PE.1	MFP15	A	LCD segment 6 output pin
	LCD_SEG7	PE.2	MFP15	A	LCD segment 7 output pin
	LCD_SEG8	PE.3	MFP15	A	LCD segment 8 output pin
	LCD_SEG9	PE.4	MFP15	A	LCD segment 9 output pin
	LCD_SEG10	PE.5	MFP15	A	LCD segment 10 output pin
	LCD_SEG11	PE.6	MFP15	A	LCD segment 11 output pin
	LCD_SEG12	PE.7	MFP15	A	LCD segment 12 output pin
	LCD_SEG13	PD.6	MFP15	A	LCD segment 13 output pin
	LCD_SEG14	PD.7	MFP15	A	LCD segment 14 output pin
	LCD_SEG15	PG.15	MFP13	A	LCD segment 15 output pin
	LCD_SEG16	PG.14	MFP15	A	LCD segment 16 output pin
	LCD_SEG17	PG.13	MFP15	A	LCD segment 17 output pin
	LCD_SEG18	PG.12	MFP15	A	LCD segment 18 output pin
	LCD_SEG19	PG.11	MFP15	A	LCD segment 19 output pin
	LCD_SEG20	PG.10	MFP15	A	LCD segment 20 output pin
	LCD_SEG21	PG.9	MFP15	A	LCD segment 21 output pin
	LCD_SEG22	PE.15	MFP15	A	LCD segment 22 output pin
	LCD_SEG23	PE.14	MFP15	A	LCD segment 23 output pin
	LCD_SEG24	PA.0	MFP11	A	LCD segment 24 output pin
	LCD_SEG25	PA.1	MFP11	A	LCD segment 25 output pin
	LCD_SEG26	PA.2	MFP11	A	LCD segment 26 output pin
	LCD_SEG27	PA.3	MFP11	A	LCD segment 27 output pin
	LCD_SEG28	PA.4	MFP15	A	LCD segment 28 output pin
	LCD_SEG29	PA.5	MFP15	A	LCD segment 29 output pin
	LCD_SEG30	PE.10	MFP15	A	LCD segment 30 output pin

Group	Pin Name	GPIO	MFP	Type	Description
	LCD_SEG31	PE.9	MFP15	A	LCD segment 31 output pin
	LCD_SEG32	PE.8	MFP15	A	LCD segment 32 output pin
	LCD_SEG33	PH.7	MFP15	A	LCD segment 33 output pin
	LCD_SEG34	PH.6	MFP15	A	LCD segment 34 output pin
	LCD_SEG35	PH.5	MFP15	A	LCD segment 35 output pin
	LCD_SEG36	PH.4	MFP15	A	LCD segment 36 output pin
	LCD_SEG37	PG.4	MFP15	A	LCD segment 37 output pin
	LCD_SEG38	PG.3	MFP15	A	LCD segment 38 output pin
	LCD_SEG39	PG.2	MFP15	A	LCD segment 39 output pin
QEI0	QEI0_A	PD.11	MFP10	I	Quadrature encoder 0 phase A input
		PA.4	MFP14	I	
		PE.3	MFP11	I	
	QEI0_B	PD.10	MFP10	I	Quadrature encoder 0 phase B input
		PA.3	MFP14	I	
		PE.2	MFP11	I	
	QEI0_INDEX	PD.12	MFP10	I	Quadrature encoder 0 index input
		PA.5	MFP14	I	
		PE.4	MFP11	I	
QEI1	QEI1_A	PA.9	MFP10	I	Quadrature encoder 1 phase A input
		PA.13	MFP12	I	
		PE.6	MFP11	I	
	QEI1_B	PA.8	MFP10	I	Quadrature encoder 1 phase B input
		PA.14	MFP12	I	
		PE.5	MFP11	I	
	QEI1_INDEX	PA.10	MFP10	I	Quadrature encoder 1 index input
		PA.12	MFP12	I	
		PE.7	MFP11	I	
QSPI0	QSPI0_CLK	PF.2	MFP5	I/O	Quad SPI0 serial clock pin.
		PA.2	MFP3	I/O	
		PC.2	MFP4	I/O	
		PH.8	MFP3	I/O	
	QSPI0_MISO0	PA.1	MFP3	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
		PC.1	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.1	MFP3	I/O	
	QSPI0_MISO1	PB.1	MFP15	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
		PA.5	MFP3	I/O	
		PC.5	MFP4	I/O	
		PH.10	MFP3	I/O	
	QSPI0_MOSI0	PA.0	MFP3	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
		PC.0	MFP4	I/O	
		PE.0	MFP3	I/O	
	QSPI0_MOSI1	PB.0	MFP15	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
		PA.4	MFP3	I/O	
		PC.4	MFP4	I/O	
		PH.11	MFP3	I/O	
	QSPI0_SS	PA.3	MFP3	I/O	Quad SPI0 slave select pin.
		PC.3	MFP4	I/O	
		PH.9	MFP3	I/O	
SC0	SC0_CLK	PB.5	MFP9	O	Smart Card 0 clock pin.
		PF.6	MFP3	O	
		PA.0	MFP6	O	
		PE.2	MFP6	O	
	SC0_DAT	PB.4	MFP9	I/O	Smart Card 0 data pin.
		PF.7	MFP3	I/O	
		PA.1	MFP6	I/O	
		PE.3	MFP6	I/O	
	SC0_PWR	PB.2	MFP9	O	Smart Card 0 power pin.
		PF.9	MFP3	O	
		PA.3	MFP6	O	
		PE.5	MFP6	O	
	SC0_RST	PB.3	MFP9	O	Smart Card 0 reset pin.
		PF.8	MFP3	O	
		PA.2	MFP6	O	
		PE.4	MFP6	O	
	SC0_nCD	PC.12	MFP9	I	Smart Card 0 card detect pin.
		PF.10	MFP3	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PA.4	MFP6	I	
		PE.6	MFP6	I	
SC1	SC1_CLK	PC.0	MFP5	O	Smart Card 1 clock pin.
		PD.4	MFP8	O	
		PB.12	MFP3	O	
	SC1_DAT	PC.1	MFP5	I/O	Smart Card 1 data pin.
		PD.5	MFP8	I/O	
		PB.13	MFP3	I/O	
	SC1_PWR	PC.3	MFP5	O	Smart Card 1 power pin.
		PD.7	MFP8	O	
		PB.15	MFP3	O	
	SC1_RST	PC.2	MFP5	O	Smart Card 1 reset pin.
		PD.6	MFP8	O	
		PB.14	MFP3	O	
	SC1_nCD	PC.4	MFP5	I	Smart Card 1 card detect pin.
		PD.3	MFP8	I	
		PD.14	MFP4	I	
SC2	SC2_CLK	PA.8	MFP3	O	Smart Card 2 clock pin.
		PA.6	MFP6	O	
		PD.0	MFP7	O	
		PA.15	MFP7	O	
		PE.0	MFP4	O	
	SC2_DAT	PA.9	MFP3	I/O	Smart Card 2 data pin.
		PA.7	MFP6	I/O	
		PD.1	MFP7	I/O	
		PA.14	MFP7	I/O	
		PE.1	MFP4	I/O	
	SC2_PWR	PA.11	MFP3	O	Smart Card 2 power pin.
		PC.7	MFP6	O	
		PD.3	MFP7	O	
		PA.12	MFP7	O	
		PH.8	MFP4	O	
	SC2_RST	PA.10	MFP3	O	Smart Card 2 reset pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PC.6	MFP6	O	
		PD.2	MFP7	O	
		PA.13	MFP7	O	
		PH.9	MFP4	O	
	SC2_nCD	PC.13	MFP3	I	Smart Card 2 card detect pin.
		PA.5	MFP6	I	
		PH.10	MFP4	I	
SD0	SD0_CLK	PB.1	MFP3	O	SD/SDIO0 clock output pin
		PE.6	MFP3	O	
	SD0_CMD	PB.0	MFP3	I/O	SD/SDIO0 command/response pin
		PE.7	MFP3	I/O	
	SD0_DAT0	PB.2	MFP3	I/O	SD/SDIO0 data line bit 0.
		PE.2	MFP3	I/O	
	SD0_DAT1	PB.3	MFP3	I/O	SD/SDIO0 data line bit 1.
		PE.3	MFP3	I/O	
	SD0_DAT2	PB.4	MFP3	I/O	SD/SDIO0 data line bit 2.
		PE.4	MFP3	I/O	
	SD0_DAT3	PB.5	MFP3	I/O	SD/SDIO0 data line bit 3.
		PE.5	MFP3	I/O	
	SD0_nCD	PB.12	MFP9	I	SD/SDIO0 card detect input pin
SPI0	SPI0_CLK	PF.8	MFP5	I/O	SPI0 serial clock pin.
		PA.2	MFP4	I/O	
		PD.2	MFP4	I/O	
		PB.14	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I^2S master clock output pin
		PF.10	MFP5	I/O	
		PA.4	MFP4	I/O	
		PD.14	MFP6	I/O	
		PB.11	MFP9	I/O	
	SPI0_MISO	PF.7	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PA.1	MFP4	I/O	
		PD.1	MFP4	I/O	
		PB.13	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SPI0_MOSI	PF.6	MFP5	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PA.0	MFP4	I/O	
		PD.0	MFP4	I/O	
		PB.12	MFP4	I/O	
	SPI0_SS	PF.9	MFP5	I/O	SPI0 slave select pin.
		PA.3	MFP4	I/O	
		PD.3	MFP4	I/O	
		PB.15	MFP4	I/O	
SPI1	SPI1_CLK	PB.3	MFP5	I/O	SPI1 serial clock pin.
		PH.6	MFP3	I/O	
		PA.7	MFP4	I/O	
		PC.1	MFP7	I/O	
		PD.5	MFP5	I/O	
		PH.8	MFP6	I/O	
	SPI1_I2SMCLK	PB.1	MFP5	I/O	SPI1 I^2S master clock output pin
		PA.5	MFP4	I/O	
		PC.4	MFP7	I/O	
		PH.10	MFP6	I/O	
	SPI1_MISO	PB.5	MFP5	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PH.4	MFP3	I/O	
		PC.7	MFP4	I/O	
		PC.3	MFP7	I/O	
		PD.7	MFP5	I/O	
		PE.1	MFP6	I/O	
	SPI1_MOSI	PB.4	MFP5	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PH.5	MFP3	I/O	
		PC.6	MFP4	I/O	
		PC.2	MFP7	I/O	
		PD.6	MFP5	I/O	
		PE.0	MFP6	I/O	
	SPI1_SS	PB.2	MFP5	I/O	SPI1 slave select pin.
		PH.7	MFP3	I/O	
		PA.6	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PC.0	MFP7	I/O	
		PD.4	MFP5	I/O	
		PH.9	MFP6	I/O	
SPI2	SPI2_CLK	PA.10	MFP4	I/O	SPI2 serial clock pin.
		PG.3	MFP3	I/O	
		PE.8	MFP5	I/O	
		PA.13	MFP5	I/O	
	SPI2_I2SMCLK	PB.0	MFP4	I/O	SPI2 I^2S master clock output pin
		PC.13	MFP4	I/O	
		PE.12	MFP5	I/O	
	SPI2_MISO	PA.9	MFP4	I/O	SPI2 MISO (Master In, Slave Out) pin.
		PG.4	MFP3	I/O	
		PE.9	MFP5	I/O	
		PA.14	MFP5	I/O	
	SPI2_MOSI	PA.8	MFP4	I/O	SPI2 MOSI (Master Out, Slave In) pin.
		PF.11	MFP3	I/O	
		PE.10	MFP5	I/O	
		PA.15	MFP5	I/O	
	SPI2_SS	PA.11	MFP4	I/O	SPI2 slave select pin.
		PG.2	MFP3	I/O	
		PE.11	MFP5	I/O	
		PA.12	MFP5	I/O	
SPI3	SPI3_CLK	PC.10	MFP6	I/O	SPI3 serial clock pin.
		PE.4	MFP5	I/O	
		PB.11	MFP11	I/O	
	SPI3_I2SMCLK	PB.1	MFP6	I/O	SPI3 I^2S master clock output pin
		PF.6	MFP9	I/O	
		PE.6	MFP5	I/O	
		PD.14	MFP3	I/O	
	SPI3_MISO	PC.12	MFP6	I/O	SPI3 MISO (Master In, Slave Out) pin.
		PE.3	MFP5	I/O	
		PB.9	MFP11	I/O	
	SPI3_MOSI	PC.11	MFP6	I/O	SPI3 MOSI (Master Out, Slave In) pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PE.2	MFP5	I/O	
		PB.8	MFP11	I/O	
	SPI3_SS	PC.9	MFP6	I/O	SPI3 slave select pin.
		PE.5	MFP5	I/O	
		PB.10	MFP11	I/O	
TAMPER0	TAMPER0	PF.6	MFP10	I/O	TAMPER detector loop pin 0.
TAMPER1	TAMPER1	PF.7	MFP10	I/O	TAMPER detector loop pin 1.
TAMPER2	TAMPER2	PF.8	MFP10	I/O	TAMPER detector loop pin 2.
TAMPER3	TAMPER3	PF.9	MFP10	I/O	TAMPER detector loop pin 3.
TAMPER4	TAMPER4	PF.10	MFP10	I/O	TAMPER detector loop pin 4.
TAMPER5	TAMPER5	PF.11	MFP10	I/O	TAMPER detector loop pin 5.
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
		PG.2	MFP13	I/O	
		PC.7	MFP14	I/O	
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PG.3	MFP13	I/O	
		PC.6	MFP14	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output pin.
		PB.14	MFP13	I/O	
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output pin.
		PG.4	MFP13	I/O	
		PA.7	MFP14	I/O	
		PD.0	MFP14	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PF.11	MFP13	I/O	
		PA.6	MFP14	I/O	
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
TM4	TM4	PB.3	MFP13	I/O	Timer4 event counter input/toggle output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PG.4	MFP12	I/O	
		PA.7	MFP10	I/O	
	TM4_EXT	PA.9	MFP12	I/O	Timer4 external capture input/toggle output pin.
		PB.13	MFP14	I/O	
TM5	TM5	PB.2	MFP13	I/O	Timer5 event counter input/toggle output pin.
		PF.11	MFP12	I/O	
		PA.6	MFP10	I/O	
	TM5_EXT	PA.8	MFP12	I/O	Timer5 external capture input/toggle output pin.
		PB.12	MFP14	I/O	
TRACE	TRACE_CLK	PE.12	MFP14	O	ETM Trace Clock output pin
	TRACE_DATA0	PE.11	MFP14	O	ETM Trace Data 0 output pin
	TRACE_DATA1	PE.10	MFP14	O	ETM Trace Data 1 output pin
	TRACE_DATA2	PE.9	MFP14	O	ETM Trace Data 2 output pin
	TRACE_DATA3	PE.8	MFP14	O	ETM Trace Data 3 output pin
UART0	UART0_RXD	PC.11	MFP3	I	UART0 data receiver input pin.
		PF.2	MFP3	I	
		PA.6	MFP7	I	
		PA.4	MFP11	I	
		PA.0	MFP7	I	
		PF.1	MFP4	I	
		PD.2	MFP9	I	
		PA.15	MFP3	I	
		PH.11	MFP8	I	
		PB.12	MFP6	I	
		PB.8	MFP5	I	
	UART0_TXD	PC.12	MFP3	O	UART0 data transmitter output pin.
		PF.3	MFP3	O	
		PA.7	MFP7	O	
		PA.5	MFP11	O	
		PA.1	MFP7	O	
		PF.0	MFP4	O	
		PD.3	MFP9	O	
		PA.14	MFP3	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PH.10	MFP8	O	
		PB.13	MFP6	O	
		PB.9	MFP5	O	
	UART0_nCTS	PC.7	MFP7	I	UART0 clear to Send input pin.
		PA.5	MFP7	I	
		PB.15	MFP6	I	
		PB.11	MFP5	I	
	UART0_nRTS	PC.6	MFP7	O	UART0 request to Send output pin.
		PA.4	MFP7	O	
		PB.14	MFP6	O	
		PB.10	MFP5	O	
UART1	UART1_RXD	PB.6	MFP6	I	UART1 data receiver input pin.
		PB.2	MFP6	I	
		PA.8	MFP7	I	
		PD.10	MFP3	I	
		PC.8	MFP8	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	
		PD.6	MFP3	I	
		PH.9	MFP10	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PD.11	MFP3	O	
		PE.13	MFP8	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PD.7	MFP3	O	
		PH.8	MFP10	O	
		PB.7	MFP6	O	
	UART1_nCTS	PE.11	MFP8	I	UART1 clear to Send input pin.
		PA.1	MFP8	I	
		PB.9	MFP6	I	
	UART1_nRTS	PE.12	MFP8	O	UART1 request to Send output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PA.0	MFP8	O	
		PB.8	MFP6	O	
UART2	UART2_RXD	PB.4	MFP12	I	UART2 data receiver input pin.
		PB.0	MFP7	I	
		PD.12	MFP7	I	
		PF.5	MFP2	I	
		PE.9	MFP7	I	
		PE.15	MFP3	I	
		PC.4	MFP8	I	
		PC.0	MFP8	I	
	UART2_TXD	PB.5	MFP12	O	UART2 data transmitter output pin.
		PB.1	MFP7	O	
		PC.13	MFP7	O	
		PF.4	MFP2	O	
		PE.8	MFP7	O	
		PE.14	MFP3	O	
		PC.5	MFP8	O	
		PC.1	MFP8	O	
	UART2_nCTS	PF.5	MFP4	I	UART2 clear to Send input pin.
		PD.9	MFP4	I	
		PC.2	MFP8	I	
	UART2_nRTS	PF.4	MFP4	O	UART2 request to Send output pin.
		PD.8	MFP4	O	
		PC.3	MFP8	O	
UART3	UART3_RXD	PC.9	MFP7	I	UART3 data receiver input pin.
		PE.11	MFP7	I	
		PC.2	MFP11	I	
		PD.0	MFP5	I	
		PE.0	MFP7	I	
		PB.14	MFP7	I	
	UART3_TXD	PC.10	MFP7	O	UART3 data transmitter output pin.
		PE.10	MFP7	O	
		PC.3	MFP11	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.1	MFP5	O	
		PE.1	MFP7	O	
		PB.15	MFP7	O	
	UART3_nCTS	PD.2	MFP5	I	UART3 clear to Send input pin.
		PH.9	MFP7	I	
		PB.12	MFP7	I	
	UART3_nRTS	PD.3	MFP5	O	UART3 request to Send output pin.
		PH.8	MFP7	O	
		PB.13	MFP7	O	
UART4	UART4_RXD	PF.6	MFP6	I	UART4 data receiver input pin.
		PC.6	MFP5	I	
		PA.2	MFP7	I	
		PC.4	MFP11	I	
		PA.13	MFP3	I	
		PH.11	MFP7	I	
		PB.10	MFP6	I	
	UART4_TXD	PF.7	MFP6	O	UART4 data transmitter output pin.
		PC.7	MFP5	O	
		PA.3	MFP7	O	
		PC.5	MFP11	O	
		PA.12	MFP3	O	
		PH.10	MFP7	O	
		PB.11	MFP6	O	
	UART4_nCTS	PC.8	MFP5	I	UART4 clear to Send input pin.
		PE.1	MFP9	I	
	UART4_nRTS	PE.13	MFP5	O	UART4 request to Send output pin.
		PE.0	MFP9	O	
UART5	UART5_RXD	PB.4	MFP7	I	UART5 data receiver input pin.
		PF.10	MFP6	I	
		PA.4	MFP8	I	
		PE.6	MFP8	I	
	UART5_TXD	PB.5	MFP7	O	UART5 data transmitter output pin.
		PF.11	MFP6	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PA.5	MFP8	O	
		PE.7	MFP8	O	
	UART5_nCTS	PB.2	MFP7	I	UART5 clear to Send input pin.
		PF.8	MFP6	I	
	UART5_nRTS	PB.3	MFP7	O	UART5 request to Send output pin.
		PF.9	MFP6	O	
USB	USB_D+	PA.14	MFP14	A	USB differential signal D+.
	USB_D-	PA.13	MFP14	A	USB differential signal D-.
	USB_OTG_ID	PA.15	MFP14	I	USB_ identification.
	USB_VBUS	PA.12	MFP14	P	Power supply from USB host or HUB.
	USB_VBUS_EN	PB.6	MFP14	O	USB external VBUS regulator enable pin.
		PB.15	MFP14	O	
	USB_VBUS_ST	PD.4	MFP14	I	USB external VBUS regulator status pin.
		PB.14	MFP15	I	
		PB.7	MFP14	I	
USCI0	USCI0_CLK	PA.11	MFP6	I/O	USCI0 clock pin.
		PD.0	MFP3	I/O	
		PE.2	MFP7	I/O	
		PB.12	MFP5	I/O	
	USCI0_CTL0	PC.13	MFP6	I/O	USCI0 control 0 pin.
		PD.4	MFP3	I/O	
		PE.6	MFP7	I/O	
		PD.14	MFP5	I/O	
	USCI0_CTL1	PA.8	MFP6	I/O	USCI0 control 1 pin.
		PD.3	MFP3	I/O	
		PE.5	MFP7	I/O	
		PB.15	MFP5	I/O	
	USCI0_DAT0	PA.10	MFP6	I/O	USCI0 data 0 pin.
		PD.1	MFP3	I/O	
		PE.3	MFP7	I/O	
		PB.13	MFP5	I/O	
	USCI0_DAT1	PA.9	MFP6	I/O	USCI0 data 1 pin.
		PD.2	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.4	MFP7	I/O	
		PB.14	MFP5	I/O	
USCI1	USCI1_CLK	PB.1	MFP8	I/O	USCI1 clock pin.
		PE.12	MFP6	I/O	
		PD.7	MFP6	I/O	
		PB.8	MFP4	I/O	
	USCI1_CTL0	PB.5	MFP8	I/O	USCI1 control 0 pin.
		PE.9	MFP6	I/O	
		PD.3	MFP6	I/O	
		PB.10	MFP4	I/O	
	USCI1_CTL1	PB.4	MFP8	I/O	USCI1 control 1 pin.
		PE.8	MFP6	I/O	
		PD.4	MFP6	I/O	
		PB.9	MFP4	I/O	
	USCI1_DAT0	PB.2	MFP8	I/O	USCI1 data 0 pin.
		PE.10	MFP6	I/O	
		PD.5	MFP6	I/O	
		PB.7	MFP4	I/O	
	USCI1_DAT1	PB.6	MFP4	I/O	USCI1 data 1 pin.
		PB.3	MFP8	I/O	
		PE.11	MFP6	I/O	
		PD.6	MFP6	I/O	
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~24 MHz (high speed) crystal output pin.

5 BLOCK DIAGRAM

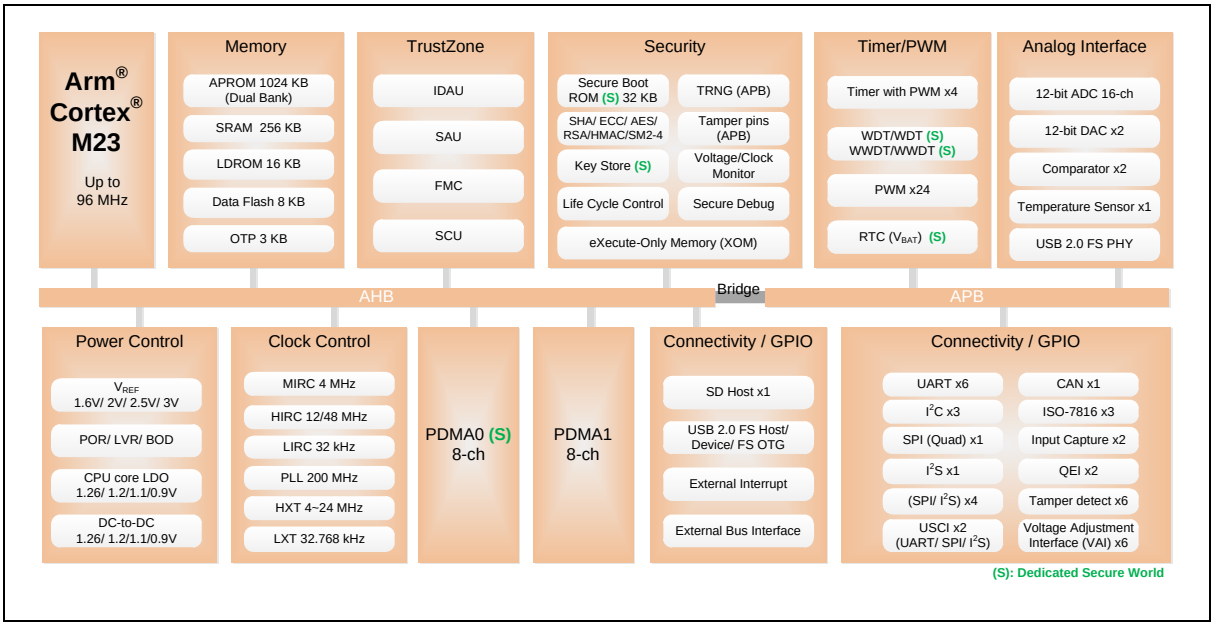


Figure 5-1 M2354 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The NuMicro® M2354 series is embedded with the Cortex®-M23 processor. The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone® technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension.Figure Figure 6.1-1 shows the functional controller of the processor.

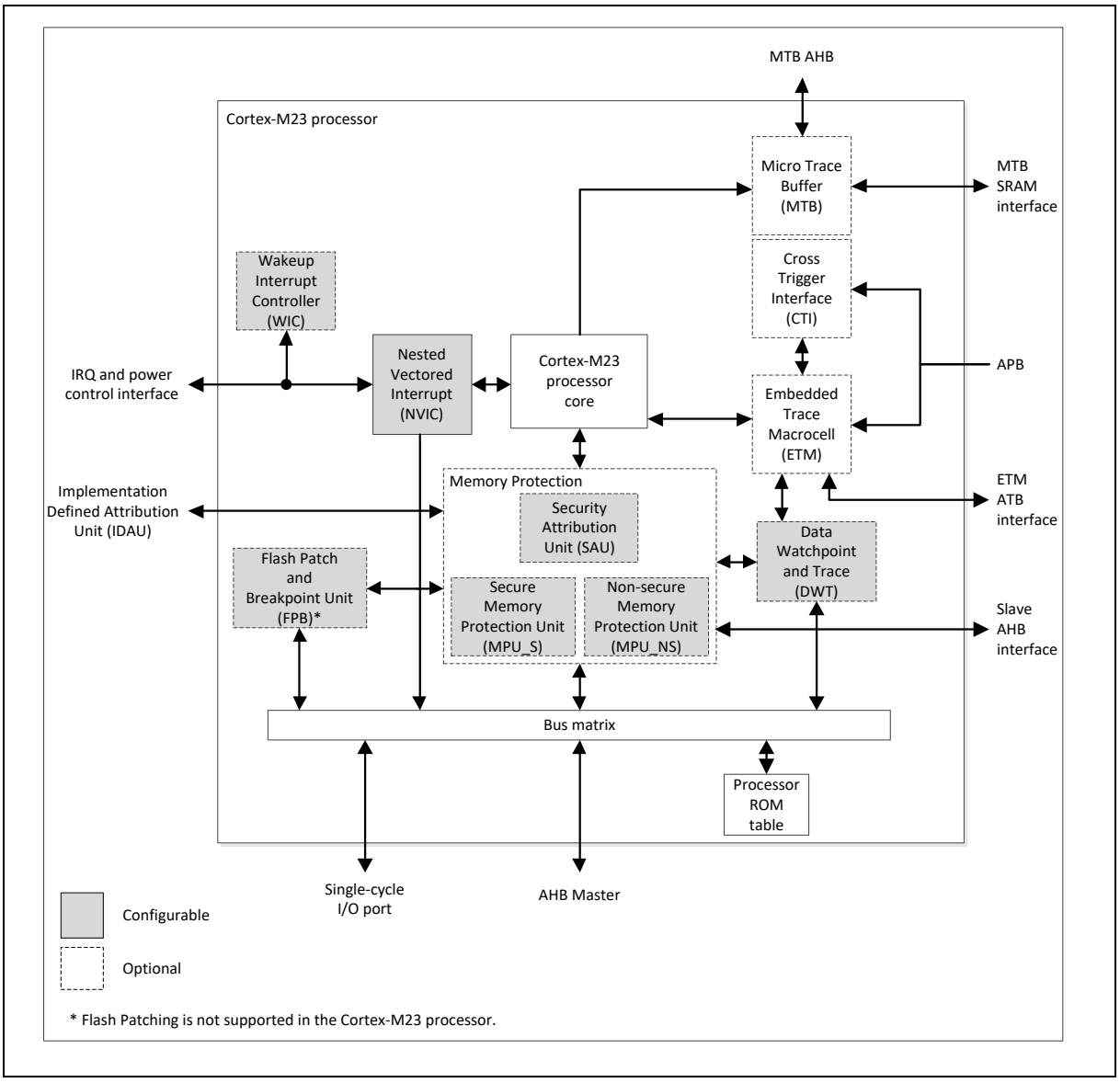


Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Protected Memory System Architecture (PMSAv8) Memory Protection Units (MPUs) for both Secure and Non-secure states.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset source are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - System Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex® -M23 core only by writing 1 to CPURST (SYS_IPRST0[1])

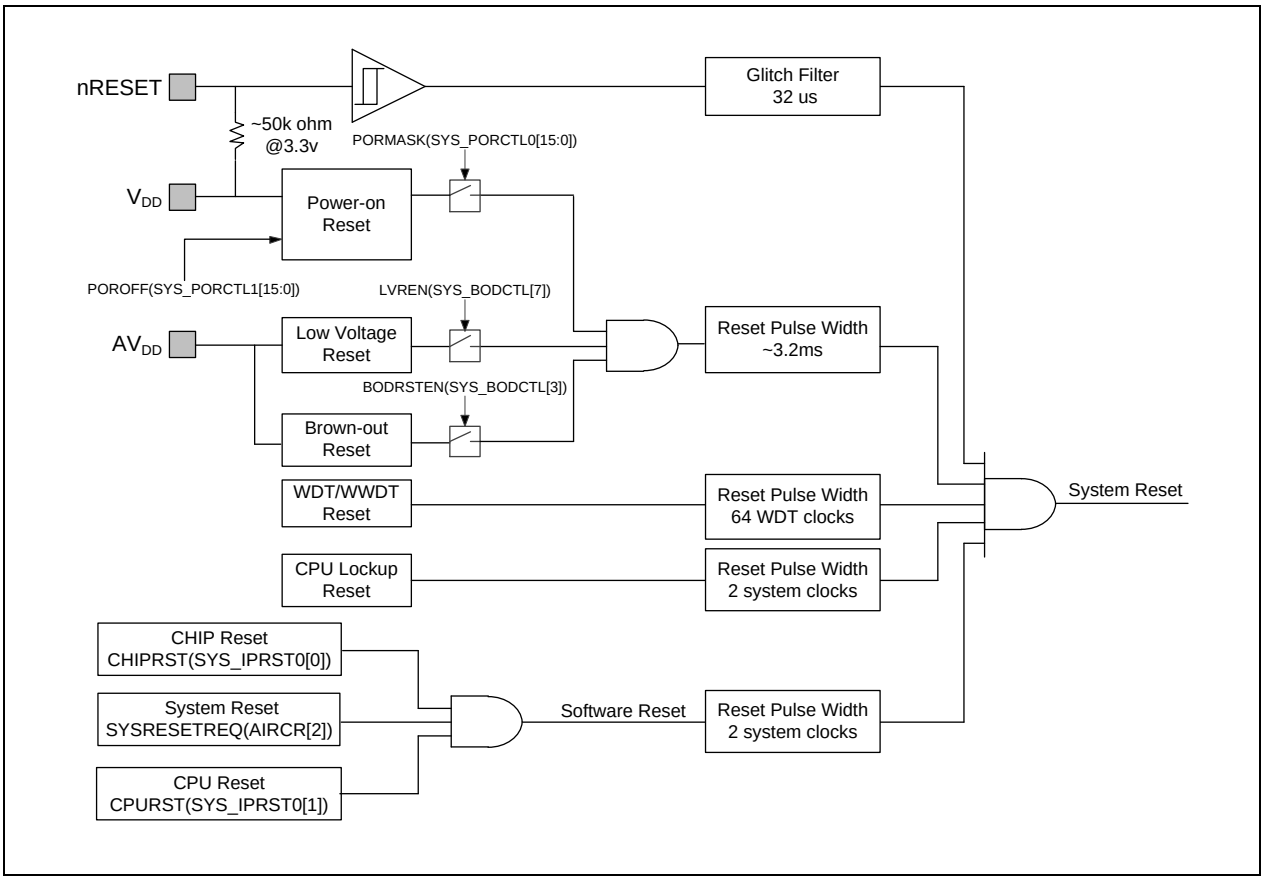


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x5 HIRC48	0x5 HIRC48	0x5 HIRC48	0x5 HIRC48	0x5 HIRC48	0x6 MIRC	0x5 HIRC48	0x6 MIRC	-
HCLKDIV (CLK_CLKDIV0[3:0])	0x0	0x0	0x0	0x0	0x0	0x3	0x0	0x3	-
PLSTATUS (SYS_PLSTS[9:8])	0x2 PL2	0x2 PL2	0x2 PL2	0x2 PL2	0x2 PL2	-	0x2 PL2	-	-
CURMVR (SYS_PLSTS[12])	0x0 LDO	-	-	-	-	-	-	-	-

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[18:16])									
BODRSTEN (SYS_BODCTL[3])									
SYS_SRAMPC0	0x0	-	-	-	-	-	-	-	-
KS (SYS_SRAMPC1[29:28])	0x0	0x0	0x0	0x0	0x0	-	0x0	-	-
RSA (SYS_SRAMPC1[27:26])	0x2	0x2	0x2	0x2	0x2	-	0x2	-	-
SYS_SRAMPC1 expect KS(bit[29:28]) and RSA(bit[27:26])	0x0800_0000	-	-	-	-	-	-	-	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[4])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
CLK_PLLCTL	0x0009_440A	0x0009_440A	0x0009_440A	0x0009_440A	0x0009_440A	0x0009_440A	0x0009_440A	0x0009_440A	-
PDMSEL (CLK_PMUCTL [2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from	Reload from	Reload from	Reload from	Reload from	-	Reload from	-	-

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
WDTEN (WDT_CTL[7])	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0		CONFIG0		
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
Other Peripheral Registers	Reset Value								-
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

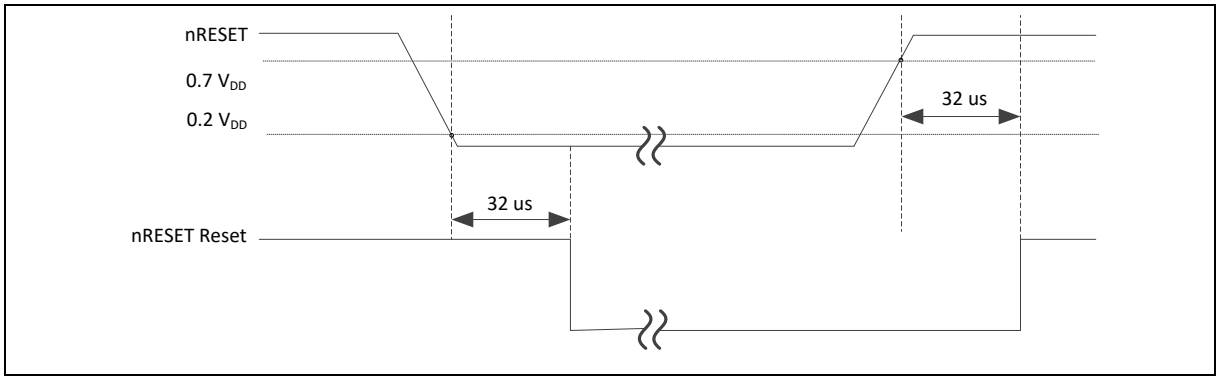


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a

POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

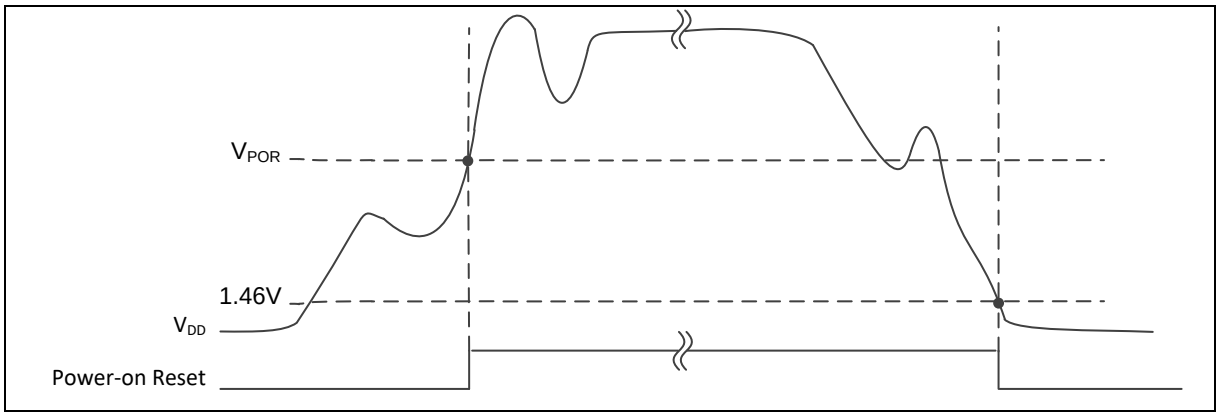


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, and wait LVR detection circuit stable flag (SYS_BODCTL[23]) to 1, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

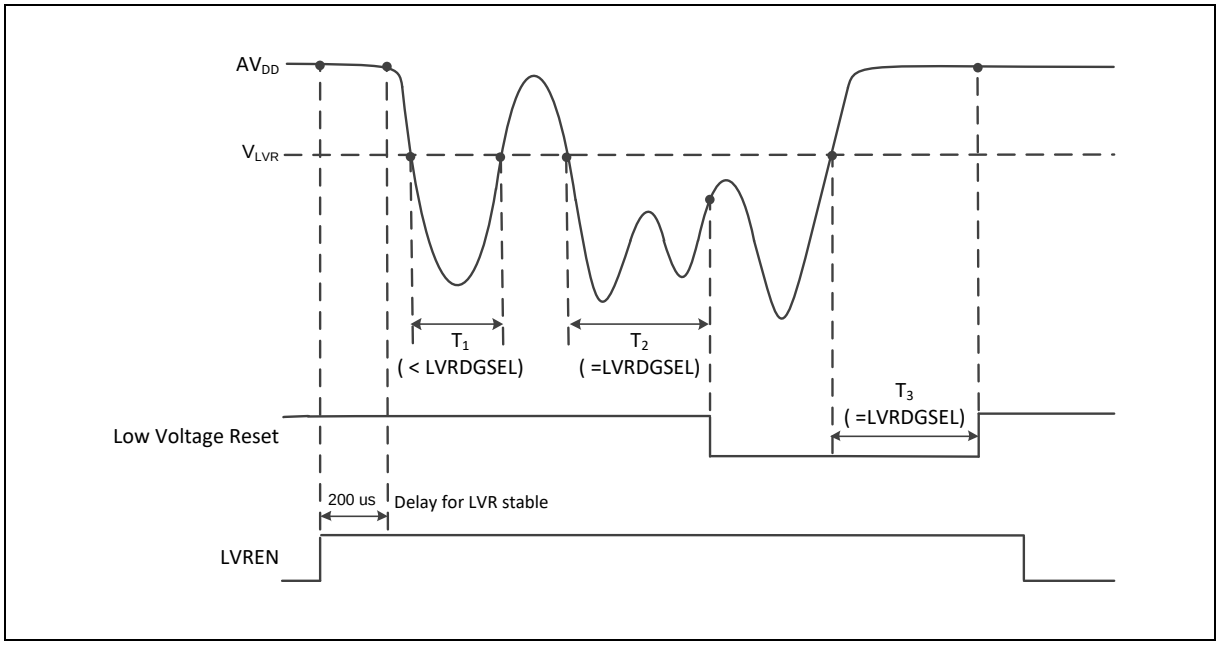


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), and wait BOD detection circuit stable flag STB(SYS_BODCTL[23]) to 1,

BOD detection circuit will be stable and the BOD function will be active. Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} that is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

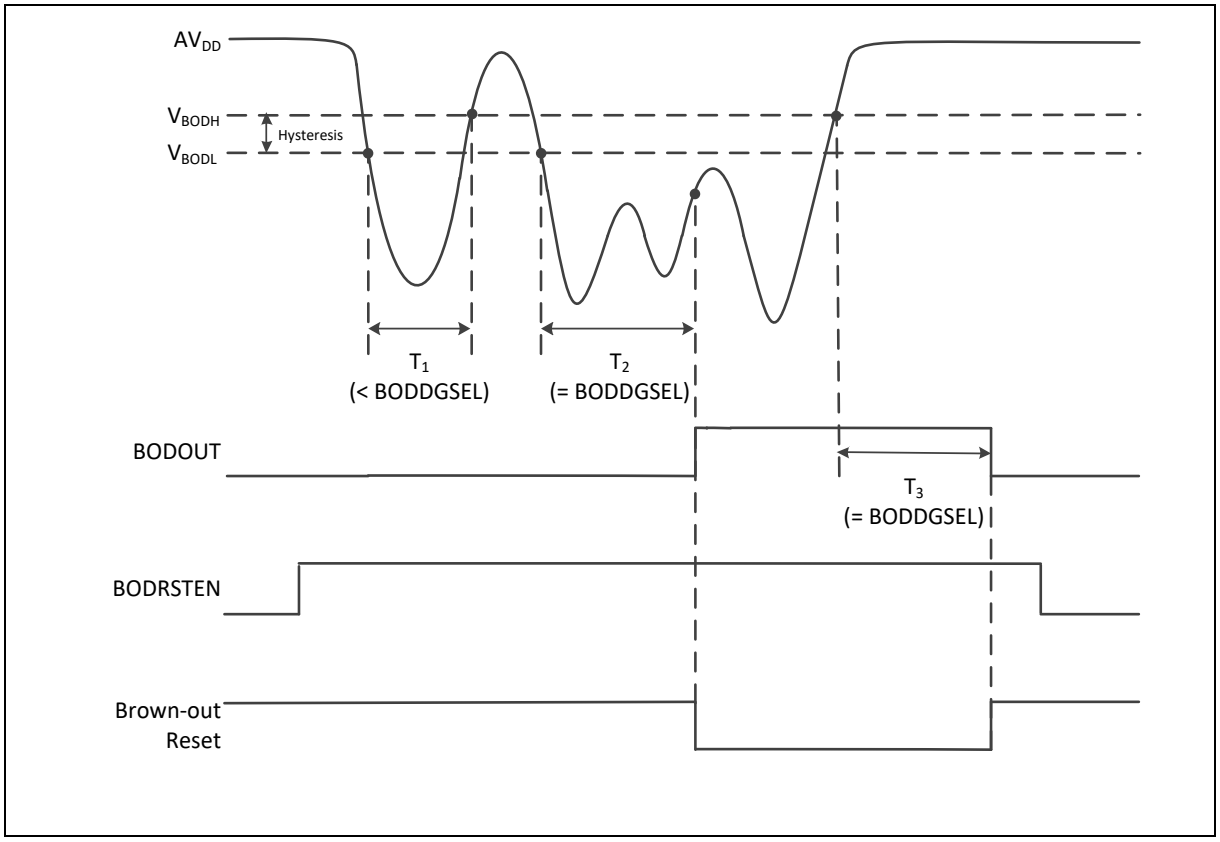


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an

unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and System Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The System Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the System Reset.

6.2.3 Power Modes and Wake-up Sources

The NuMicro® M2354 series has a power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power modes in the NuMicro® M2354 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Power level 0	96 MHz	1.26	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Power level 1	84 MHz	1.2	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Power level 2	48 MHz	1.1	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Power level 3	4 MHz	0.9	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Idle mode	CPU enter Sleep mode	keep	Only CPU clock is disabled.
Power-down mode (PD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT/MIRC, and only RTC/WDT/EWDT/Timer/UART/LCD peripheral clocks still enable if their clock sources are selected as LIRC/LXT/MIRC.
Fast Wake-up Power-down mode (FWPD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT/MIRC, and only RTC/WDT/EWDT/Timer/UART/LCD peripheral clocks still enable if their clock sources are selected as LIRC/LXT/MIRC.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT/MIRC, and only RTC/WDT/EWDT/Timer/UART/LCD peripheral clocks still enable if their clock sources are selected as LIRC/LXT/MIRC.
Ultra Low leakage Power-down mode	CPU enters Deep Sleep mode	0.8	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/EWDT/Timer/UART/LCD peripheral clocks still enable if their clock

(ULLPD)			sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	0.9 or keep	Only LIRC/LXT still enable for RTC function and wake-up timer usage.
Deep Power-down mode (DPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage.

Table 6.2-2 Power Mode Table

Each power mode has different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Ultra Low leakage Power-down mode	1	1	3	YES
Fast Wake-up Power-down mode	1	1	2	YES
Standby Power-down mode	1	1	4	YES
Deep Power-down mode	1	1	6	YES

Table 6.2-3 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, WDT, EWDT, SDH, Timer, I²C, USCI, RTC, ACMP, TAMPER and CLKD.
Available Clocks	All	All except CPU clock	LXT, LIRC and MIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

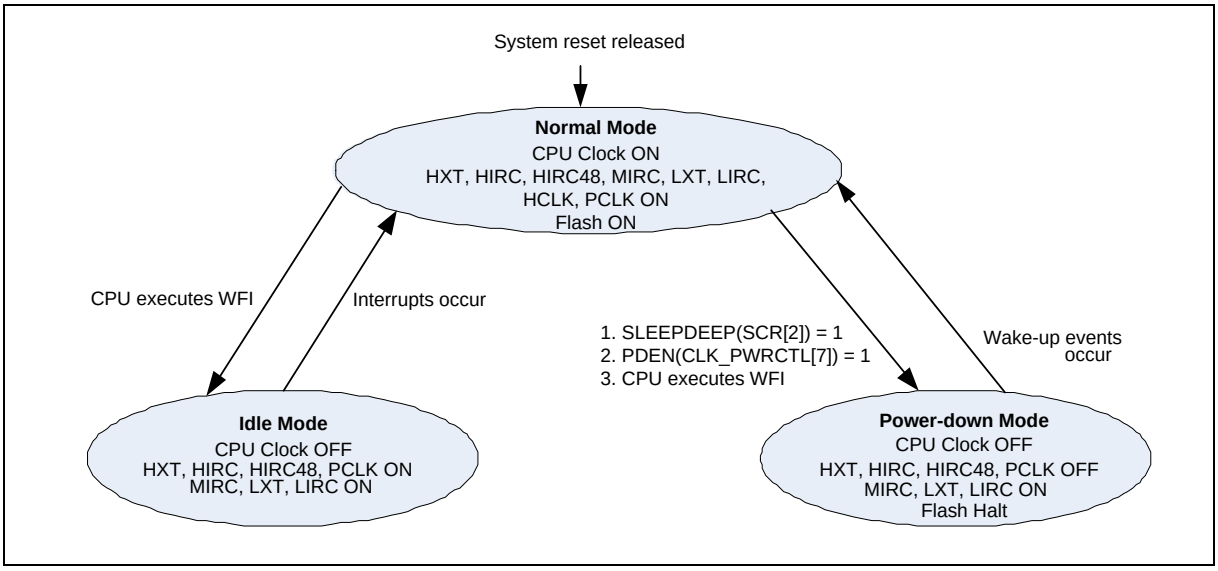


Figure 6.2-6 Power Mode State Machine

1. LXT ON or OFF depends on software setting in normal mode.
2. LIRC ON or OFF depends on software setting in normal mode.
3. MIRC ON or OFF depends on software setting in normal mode.
4. If TIMER clock source is selected as LIRC/LXT/MIRC and LIRC/LXT/MIRC is on.
5. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
6. If RTC clock source is selected as LIRC/LXT and LIRC/LXT is on.
7. If UART clock source is selected as LXT and LXT is on.
8. If LCD clock source is selected as LIRC/LXT and LIRC/LXT is on.
   If LCD charge pump clock source is selected as MIRC/MIRC1P2M and MIRC/MIRC1P2M is on.
9. If EWDT clock source is selected as LIRC/LXT and LIRC/LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode (PD/FWPD/LLPD/ULLPD)	Power-Down Mode (SPD/DPD)
HXT	ON	ON	Halt	Halt
HIRC	ON	ON	Halt	Halt
HIRC48	ON	ON	Halt	Halt
MIRC	ON	ON	ON/OFF[3]	OFF
LXT	ON	ON	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON	ON/OFF[2]	ON/OFF[2]
PLL	ON	ON	Halt	Halt
CPU	ON	Halt	Halt	Halt
HCLK/PCLK	ON	ON	Halt	Halt

FLASH	ON	ON	Halt	Halt
TIMER	ON	ON	ON/OFF[4]	Halt
WDT	ON	ON	ON/OFF[5]	Halt
RTC	ON	ON	ON/OFF[6]	ON/OFF[6]
UART	ON	ON	ON/OFF[7]	Halt
LCD	ON	ON	ON/OFF[8]	Halt
EWDT	ON	ON	ON/OFF[9]	Halt
Others	ON	ON	Halt	Halt

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, ACMP, WDT, EWDT, SDH, Timer, I²C, USCI, RTC, TAMPER and CLKD.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-down mode			System Can Enter Power-Down Mode Again Condition*
		PD LLPD ULLPD FWPD	SPD	DPD	
BOD	Brown-out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-out Detector Reset	-	V	-	After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	V	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
EINT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA6-PA15,PB~PD) Wake-up pin	rising or falling edge event, 50-pin	-	V	-	GPxWK(CLK_PMUSTS[11:8]) is cleared when SPD mode is entered.
GPIO(PC.0)	rising or falling edge event, 1-pin	-	-	V	PINWK0(CLK_PMUSTS[0]) is cleared when

Wake-up pin					DPD mode is entered.
GPIO(PB.0) Wake-up pin	rising or falling edge event, 1-pin	-	-	V	PINWK1(CLK_PMUSTS[3]) is cleared when DPD mode is entered.
GPIO(PB.2) Wake-up pin	rising or falling edge event, 1-pin	-	-	V	PINWK2(CLK_PMUSTS[4]) is cleared when DPD mode is entered.
GPIO(PB.12) Wake-up pin	rising or falling edge event, 1-pin	-	-	V	PINWK3(CLK_PMUSTS[5]) is cleared when DPD mode is entered.
GPIO(PF.6) Wake-up pin	rising or falling edge event, 1-pin	-	-	V	PINWK4(CLK_PMUSTS[6]) is cleared when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
EWDT	EWDT Interrupt	V	-	-	After software writes 1 to clear WKF (EWDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	RTC Tamper Interrupt	V	-	-	After software writes 1 to clear TAMPxIF (RTC_INTSTS[8:13]).
	Wakeup by RTC alarm	-	V	V	RTCWK (CLK_PMUSTS[2]) is cleared when DPD or SPD mode is entered.
	Wakeup by RTC tick time	-	V	V	RTCWK (CLK_PMUSTS[2]) is cleared when DPD or SPD mode is entered.
	Wakeup by tamper event	-	V	V	RTCWK (CLK_PMUSTS[2]) is cleared when DPD or SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).

USCI I²C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I²C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	1.Remote wake-up 2.Plug in wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected 3.Remote-wakeup	V	-	-	1.After write 1 to clear RHSC (HcInterruptStatus[7]). 2.After write 1 to clear RHSC (HcInterruptStatus[7]). 3.After write 1 to clear RHSC (HcInterruptStatus[7]). and port suspended.
OTG	ID pin state be change	V	-	-	After software writes 1 to set WKEN(OTG_CTL[5]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
	ACMPO status change	-	V	-	ACMPWK (CLK_PMUSTS[14]) is cleared when SPD mode is entered.
CAN	Incoming Data Toggle	V	-	-	After software writes 0 to clear WAKUP_STS (CAN_WU_STATUS[0])
SDH	Card detection	V	-	-	Clear CDIF0 (SDH_INTSTS[8]) after SDH wake-up.
TAMPER	Event detection	V	-	-	Clear TAMP_EVSTS or disable Enable in TAMP_INTEVEN after TAMPER wake-up.
	Wakeup by Event detection	-	V	-	TAMPERWK (CLK_PMUSTS[15]) is cleared when SPD mode is entered.
CLKD	LXT clock fail interrupt	V	-	-	After software writes 1 to clear LXTFIF (CLK_CLKDSTS[1]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 0.9V, 1.1V, 1.2V or 1.26V power for digital operation and I/O pins.
- USB transceiver power from V_{DD} offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the

digital power (V_{DD}). If system enters SPD mode SW_SPD switch is turned off, and internal voltage regulator can be set to LDO mode or DC-DC converter mode. Figure 6.2 7 shows the power distribution.

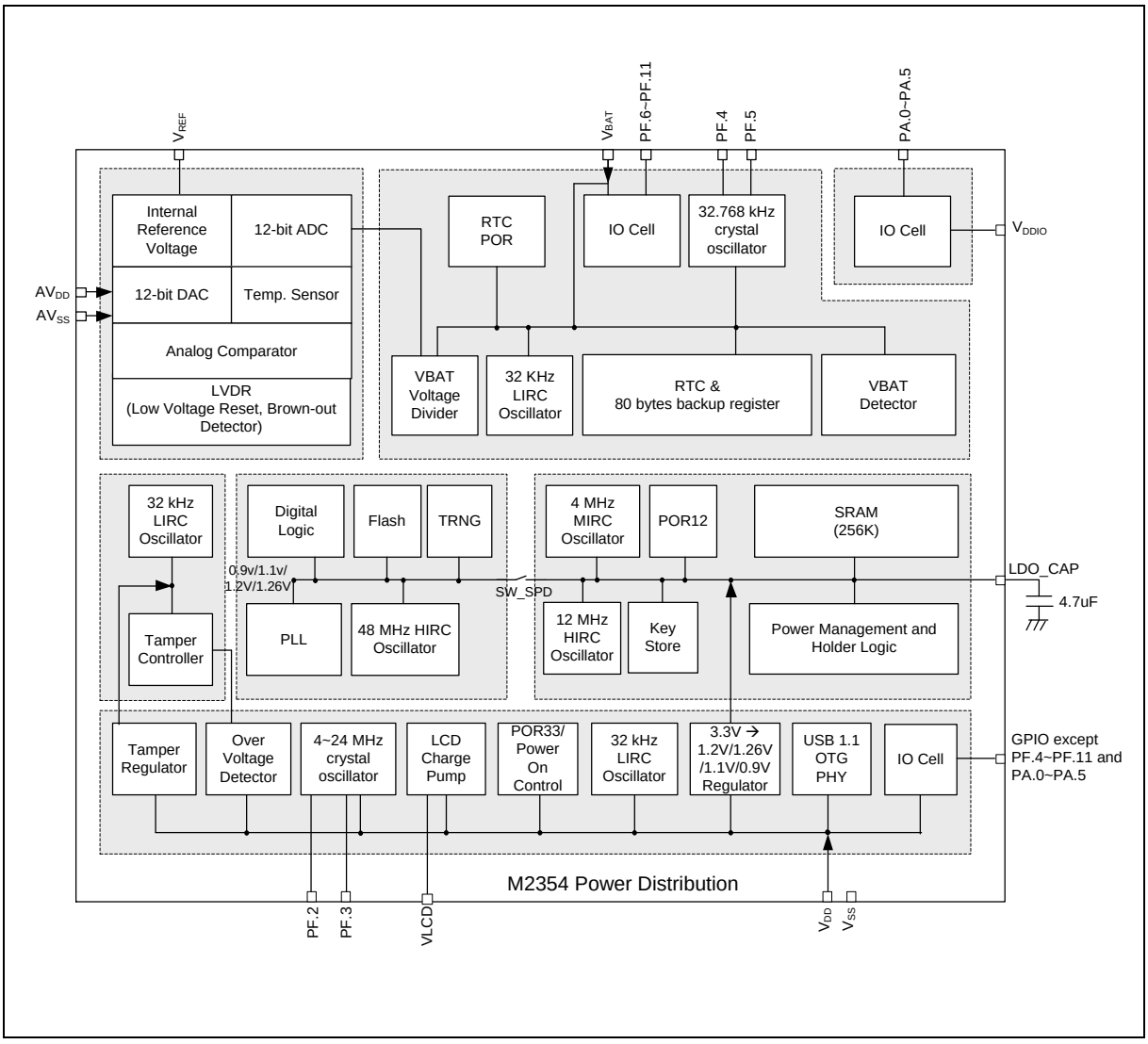


Figure 6.2-7 Power Distribution Diagram

6.2.5 Bus Matrix

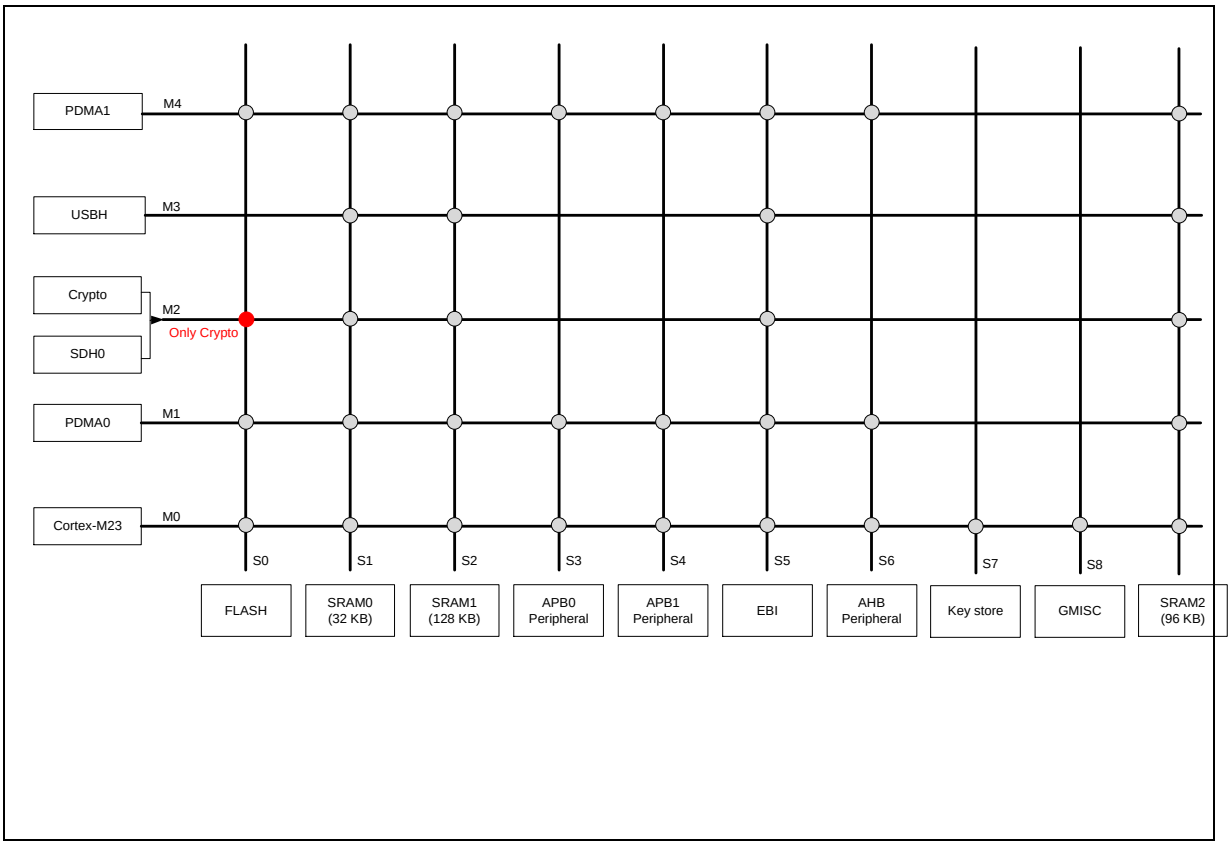


Figure 6.2-2 M2354 Bus Matrix Architecture Diagram

Refer to Figure 6.2-2. This chip uses Advanced Microcontroller Bus Architecture (AMBA) protocol to implement system bus. The system has five masters and nine slaves, in which a different master can communicate with a different slave at the same time through Bus Matrix. The Cortex®-M23 core processor acts as the master in Bus Matrix, located on M0 to communicate with any slaves through Bus Matrix. PDMA0 and PDMA1 are Peripheral Direct Memory Access and act as the master in Bus Matrix, respectively located on M1 and M4, which can communicate with any slaves through Bus Matrix. SDH0 and Crypto share the same master bandwidth located on M2. USBH acts as the master role in Bus Matrix and is located on M3. The slave AHB Peripheral is the Advanced High-performance Bus (AHB) controller, and any master can communicate with any AHB peripheral through Bus Matrix.

6.2.6 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. This chip implement Arm® TrustZone Architecture as well as memory alias technique, secure code and non-secure code can run together on the chip well, while both have different memory view. Secure code view is shown in Table 6.2-1 and non-secure code view is shown in Table 6.2-2.

The NuMicro® M2354 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		

0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 KB)
0x0000_0000 – 0x000F_FFFF	FLASH_BA	FLASH Memory Space (1024 KB)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 KB)
0x2000_8000 – 0x2002_7FFF	SRAM1_BA	SRAM Memory Space (128 KB)
0x2002_8000 – 0x2003_FFFF	SRAM2_BA	SRAM Memory Space (96 KB)
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256 MB)
Secure Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers (always secure)
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers (always secure)
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers (always secure)
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA 0 Control Registers (always secure)
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers (always secure)
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_8000 – 0x4000_8FFF	PDMA1_BA	Peripheral DMA 1 Control Registers (secure or non-secure)
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_2000 – 0x4003_4FFF	CRPT_BA	Cryptographic Accelerator Registers
0x4003_5000 – 0x4003_5FFF	KS_BA	Key Store Registers (always secure)
0x4002_F000 – 0x4002_FFFF	SCU_BA	Secure Configuration Unit Registers (always secure)
Secure APB Controllers Space (0x4004_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers (always secure)
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register (always secure)
0x4004_2000 – 0x4004_2FFF	EWDT_BA	Extra Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I2S0 Interface Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers (always secure)
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_2000 – 0x4005_2FFF	TMR45_BA	Timer4/Timer5 Control Registers

0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers
0x4006_4000 – 0x4006_4FFF	SPI3_BA	SPI3 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I2C2 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	QEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	QEI1_BA	QEI1 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400B_5000 – 0x400B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x400B_9000 – 0x400B_9FFF	TRNG_BA	TRNG Control Registers
0x400B_B000 – 0x400B_BFFF	LCD_BA	LCD Control Register
0x400B_D000 – 0x400B_DFFF	TAMPER_BA	Tamper Control Register (always secure)
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

Address Space	Token	Controllers
Non-secure Peripheral Controllers Space (0x5000_0000 – 0x500F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA_NS	System Control Registers
0x5000_4000 – 0x5000_4FFF	GPIO_BA	GPIO Control Registers
0x5000_9000 – 0x5000_9FFF	USBH_BA	USB Host Control Registers
0x5000_D000 – 0x5000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x5001_0000 – 0x5001_0FFF	EBI_BA	External Bus Interface Control Registers
0x5001_8000 – 0x5000_8FFF	PDMA1_BA	Peripheral DMA 1 Control Registers (secure or non-secure)
0x5003_1000 – 0x5003_1FFF	CRC_BA	CRC Generator Registers
0x5003_2000 – 0x5003_4FFF	CRPT_BA	Cryptographic Accelerator Registers
Non-secure APB Controllers Space (0x5004_0000 ~ 0x500F_FFFF)		
0x5004_2000 – 0x5004_2FFF	EWDT_BA	Extra Watchdog Timer Control Registers
0x5004_3000 – 0x5004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x5004_5000 – 0x5004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x5004_7000 – 0x5004_7FFF	DAC_BA	DAC Control Registers
0x5004_8000 – 0x5004_8FFF	I2S0_BA	I2S0 Interface Control Registers
0x5004_D000 – 0x5004_DFFF	OTG_BA	OTG Control Registers
0x5005_1000 – 0x5005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x5005_2000 – 0x5005_2FFF	TMR45_BA	Timer4/Timer5 Control Registers
0x5005_8000 – 0x5005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x5005_9000 – 0x5005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x5005_A000 – 0x5005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x5005_B000 – 0x5005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x5006_0000 – 0x5006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x5006_1000 – 0x5006_1FFF	SPI0_BA	SPI0 Control Registers
0x5006_2000 – 0x5006_2FFF	SPI1_BA	SPI1 Control Registers
0x5006_3000 – 0x5006_3FFF	SPI2_BA	SPI2 Control Registers
0x5006_4000 – 0x5006_4FFF	SPI3_BA	SPI3 Control Registers
0x5007_0000 – 0x5007_0FFF	UART0_BA	UART0 Control Registers
0x5007_1000 – 0x5007_1FFF	UART1_BA	UART1 Control Registers
0x5007_2000 – 0x5007_2FFF	UART2_BA	UART2 Control Registers
0x5007_3000 – 0x5007_3FFF	UART3_BA	UART3 Control Registers
0x5007_4000 – 0x5007_4FFF	UART4_BA	UART4 Control Registers
0x5007_5000 – 0x5007_5FFF	UART5_BA	UART5 Control Registers

0x5008_0000 – 0x5008_0FFF	I2C0_BA	I2C0 Control Registers
0x5008_1000 – 0x5008_1FFF	I2C1_BA	I2C1 Control Registers
0x5008_2000 – 0x5008_2FFF	I2C2_BA	I2C2 Control Registers
0x5009_0000 – 0x5009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x5009_1000 – 0x5009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x5009_2000 – 0x5009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x500A_0000 – 0x500A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x500B_0000 – 0x500B_0FFF	QEI0_BA	QEI0 Control Registers
0x500B_1000 – 0x500B_1FFF	QEI1_BA	QEI1 Control Registers
0x500B_4000 – 0x500B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x500B_5000 – 0x500B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x500B_9000 – 0x500B_9FFF	TRNG_BA	TRNG Control Registers
0x400B_B000 – 0x400B_BFFF	LCD_BA	LCD Control Register
0x500C_0000 – 0x500C_0FFF	USBD_BA	USB Device Control Register
0x500D_0000 – 0x500D_0FFF	USCI0_BA	USCI0 Control Registers
0x500D_1000 – 0x500D_1FFF	USCI1_BA	USCI1 Control Registers

Table 6.2-2 Non-secure Address Space Assignments for On-Chip Controllers

6.2.7 Implementation Defined Attribution Unit (IDAU)

6.2.7.1 Overview

The Arm®v8-M has the new feature called TrustZone®, which adds an additional security state to allow full isolation of two security levels. The processor security state is decided by the memory definition. For example, processor is in Secure state when the code is executed in the Secure region. The memory map security state will be defined by the combination of:

- Internal Security Attribution Unit (SAU)
- Implementation Defined Attribution Unit (IDAU)

These attribution units define the memory space into four type regions:

- Secure Region: contains Secure program code or data
- Non-secure Callable Region (NSC): contains entry functions for Non-secure programs to access Secure functions
- Non-secure Region: contains Non-secure program code or data
- Exempt Region: exempt region will be exempted from security check

For each memory region defined by the SAU and IDAU has a region number generated by the SAU or by the IDAU. Region number is used for determining a group of memory share the same security attribute. Overlapping region numbers are not allow. For testing security attributes and region numbers, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine that the memory range is located entirely in same space. To be more specific, please refer to the Arm®v8-M Architecture Reference Manual. The M2354 IDAU memory map attributions and corresponding region numbers are shown in Figure 6.2-8. The address from 0xE000_0000 to

0xFFFF_FFFF is marked as exempt regions because the behavior of the address is fixed, so their security attributes do not control by the SAU or IDAU.

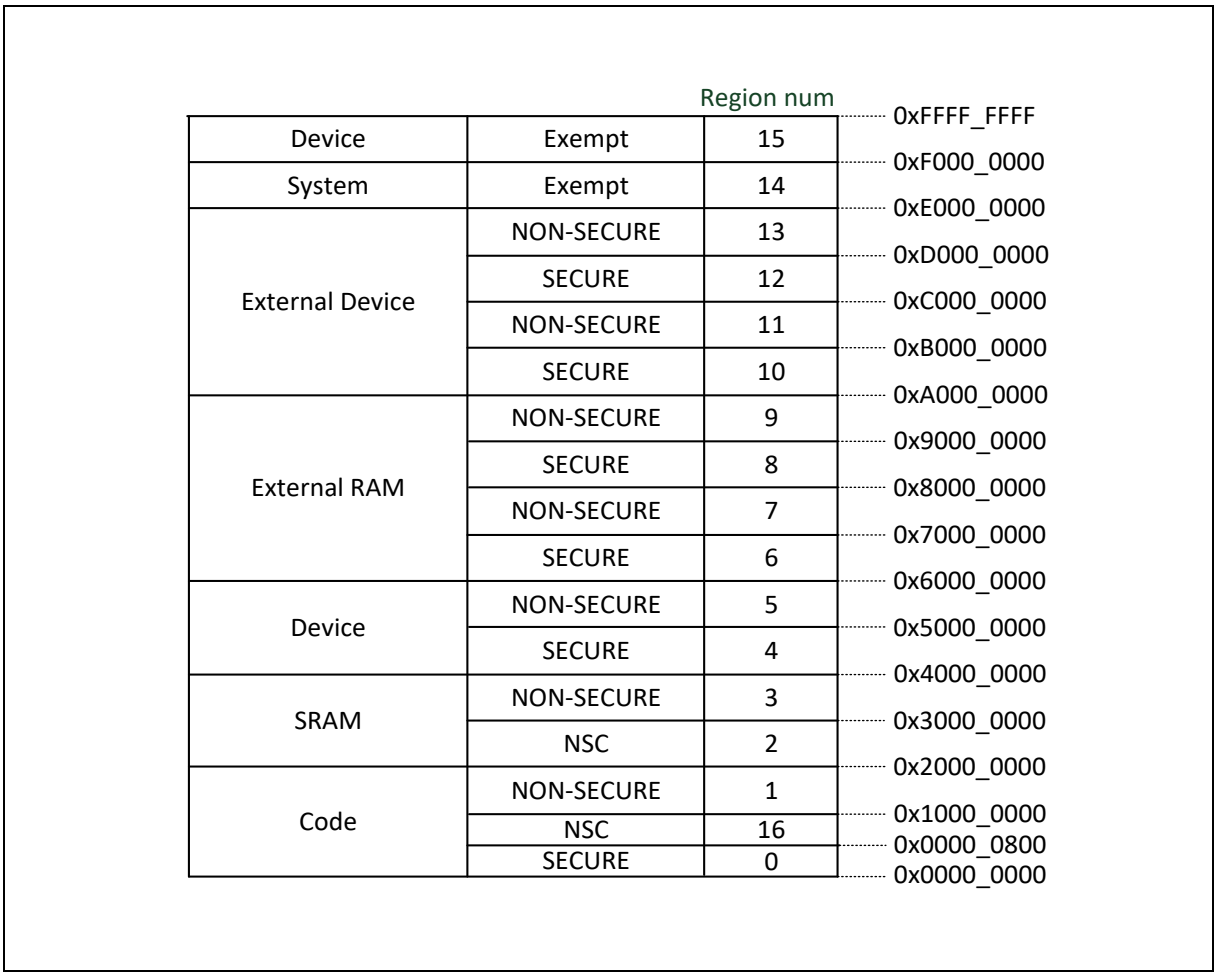


Figure 6.2-8 IDAU Memory Map

6.2.7.2 IDAU Block Diagram

The IDAU block diagram is shown in Figure 6.2-9. IDAU is security attribute unit connected outside of the processor. Both SAU and IDAU are responsible to response the security property of the address from processor, the only difference is that the memory security attribute of the SAU is configurable and the IDAU is fixed. After the processor compares the security property of the IDAU and SAU, it will take the highest security attribute applied. The hierarchy of security levels from high to low is: Secure > NSC > Non-secure.

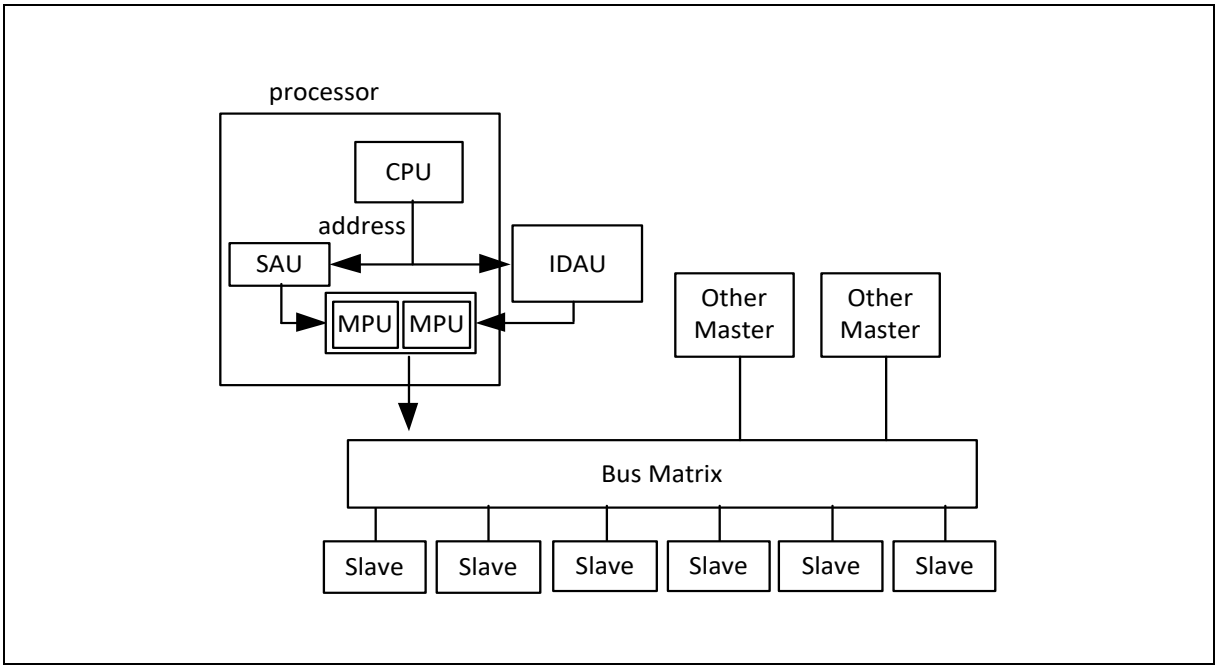


Figure 6.2-9 IDAU Block Diagram

6.2.8 SRAM Memory Organization

This chip supports embedded SRAM with a total of 256 Kbytes size and the SRAM organization is separated into three banks: SRAM bank0, SRAM bank1, and SRAM bank2. The first bank has 32 Kbytes address space, the second bank has 128Kbyte address space, and the third bank has 96Kbyte address space. These three banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure the chip is operating more stable.

- Supports total 256 Kbytes SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0
- Supports oversize response error

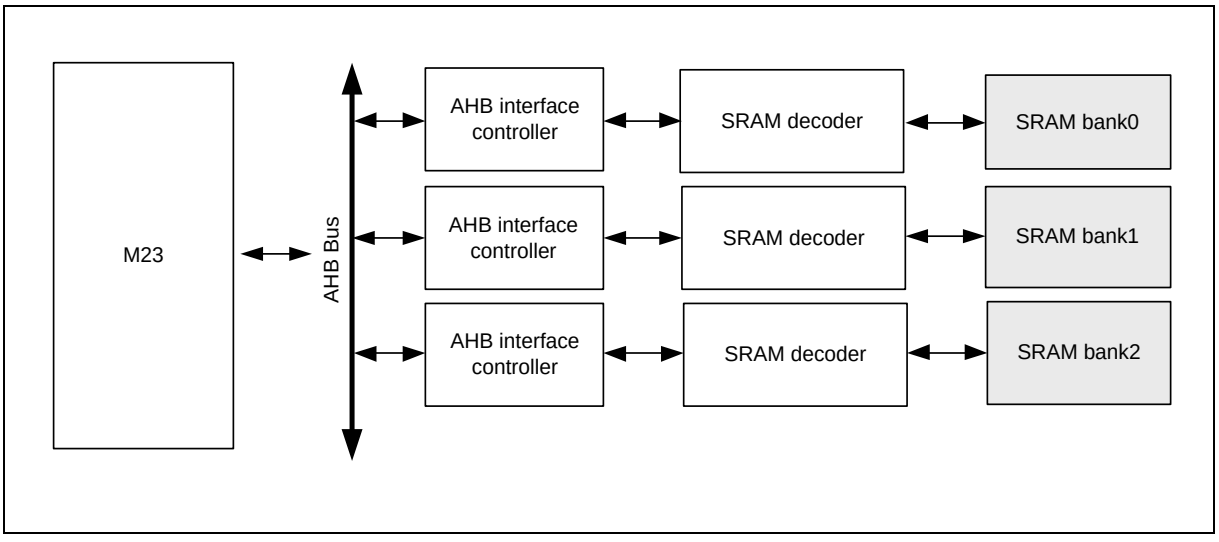


Figure 6.2-10 SRAM Block Diagram

Figure 6.2-11 shows the SRAM organization. There are three SRAM banks. The bank0 is addressed to 32 Kbytes, the bank1 is addressed to 128 Kbytes and the bank2 is addressed to 96 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF(Secure) or 0x3000_0000 to 0x3000_7FFF(Non-secure). The bank1 address space is from 0x2000_8000 to 0x2002_7FFF (Secure) or 0x3000_8000 to 0x3002_7FFF (Non-secure). The bank2 address space is from 0x2002_8000 to 0x2003_FFFF (Secure) or 0x3002_8000 to 0x3003_FFFF (Non-secure). The address between 0x2004_0000 to 0x2FFF_FFFF(Secure) and 0x3004_0000 to 0x3FFF_FFFF(Non-secure) is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

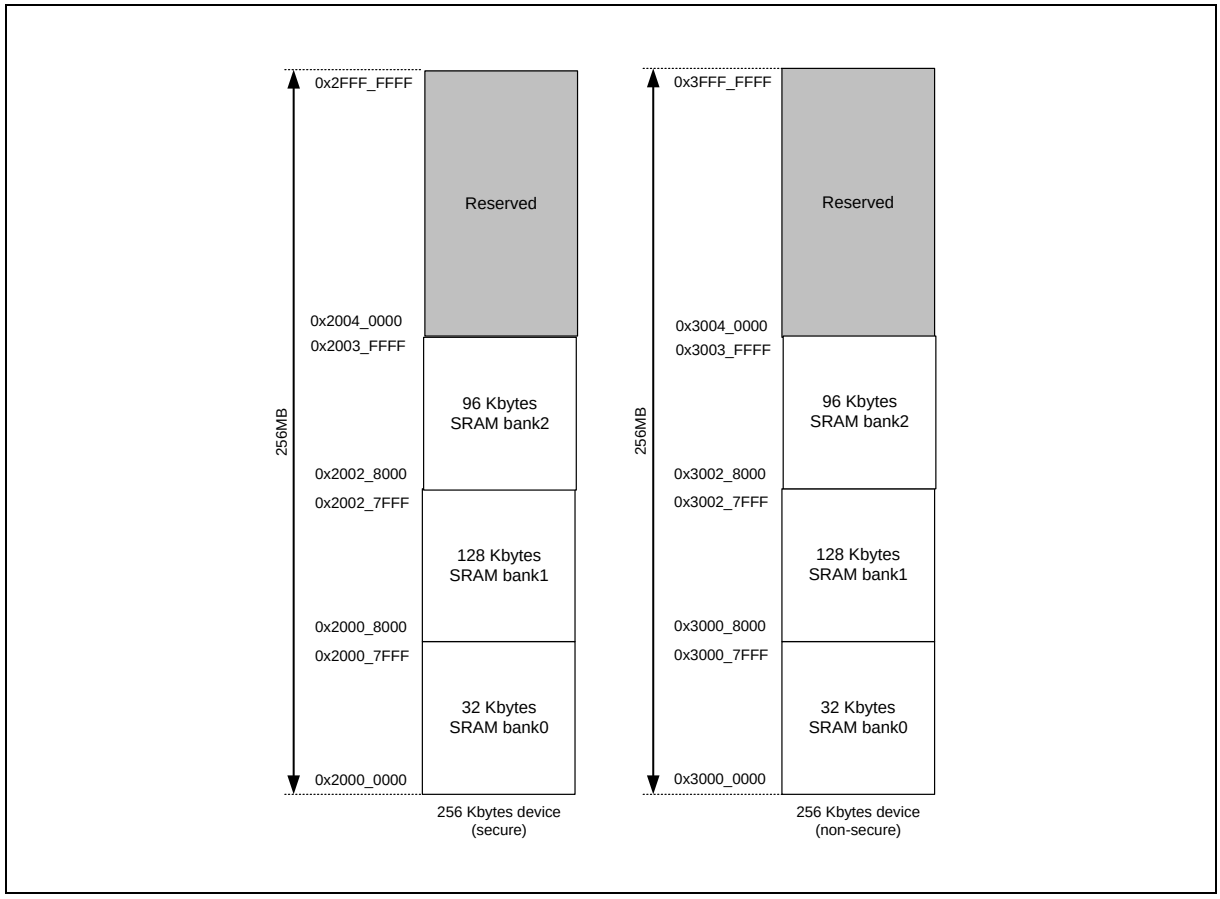


Figure 6.2-11 SRAM Memory Organization

The SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurs, the PERRIF (SYS_SRAMSTS[0]) will be asserted to 1 and the SYS_SRAMEADR register will recode the address with the parity error. Chip will enter interrupt when SRAM parity error occurs if PERRIEN (SYS_SRAMICTL[0]) is set to 1. When SRAM parity error occurs, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAMSTS[0]) bit.

SRAM Power Control

The SRAM bank0 and bank1, and bank2 have marco retention and power shut down function. Each SRAM marco can be configured to retention or power shut down mode independently by SRAMxPMn(SYS_SRAMPC0 and SYS_SRAMPC1, x=0-2 n=0-7). Figure 6.2-12 shows the SRAM marco number in bank0, bank1 and bank2. When chip power down wake up, the SRAM marcos wake up in the order of marco number, from SRAM marco0 to SRAM marco17.

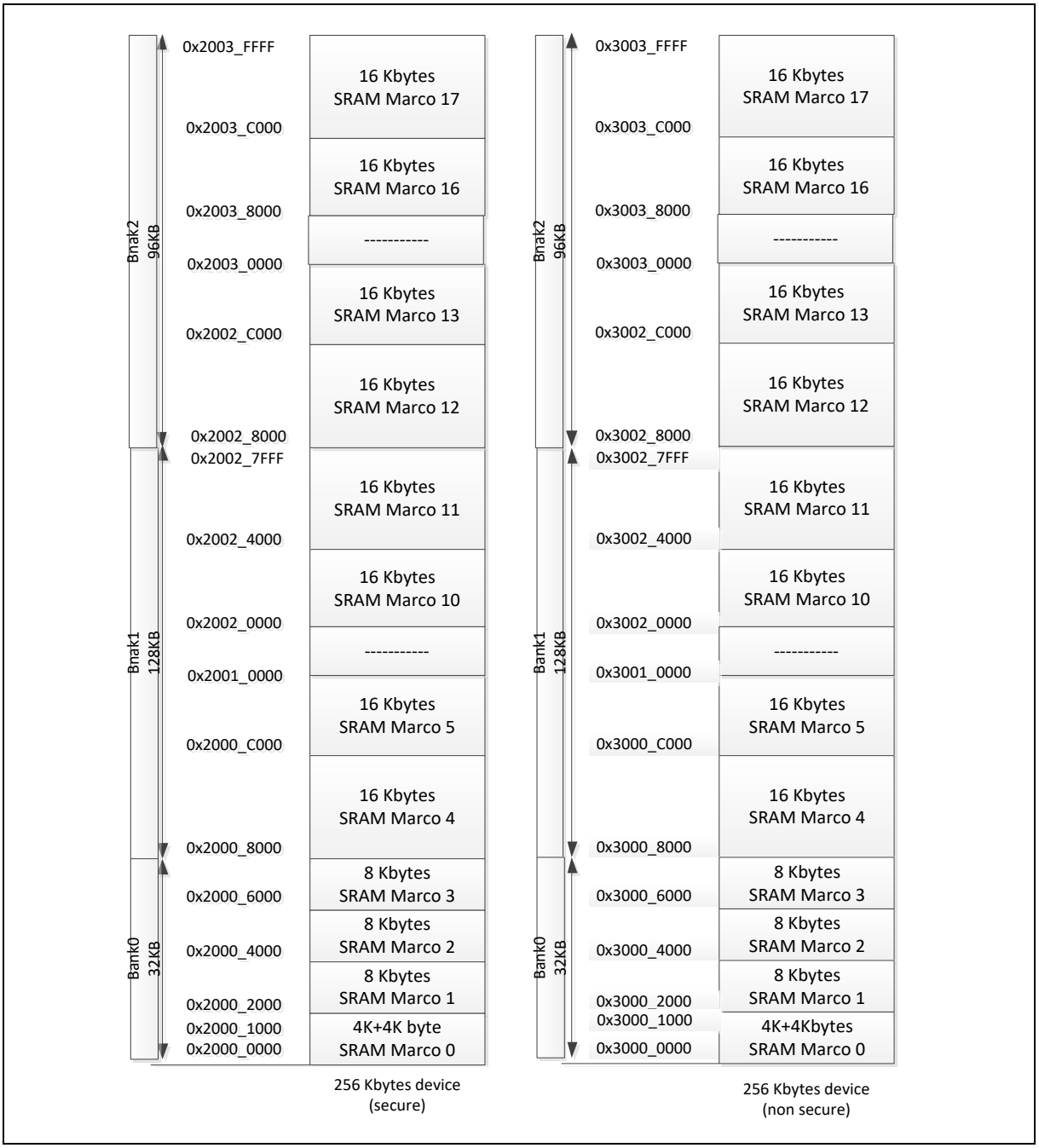


Figure 6.2-12 SRAM Marco Organization

For system SRAM (bank0, bank1, and bank2) and Key store SRAM, if the SRAM power mode is set to normal mode, it automatically changes to retention mode when system enters PD/LLPD/ULLPD/SPD Power-down mode, and then changes back to normal mode after wake-up. System and Key store SRAM power mode do not change when system enters FWPD Power-down mode. When system enters DPD Power-down mode, system and Key store SRAM is always operating in power shut down mode and reset to normal mode after wake-up.

For other peripheral SRAM, when system enters PD/LLPD/ULLPD/SPD Power-down mode, if peripheral SRAM power mode is set to normal mode, the peripheral SRAM power mode automatically changes to retention mode, and then changes back to normal mode after wake-up, too.

But if entering SPD Power-down mode, peripheral SRAM resets to default power mode after wake-up.

When system enters DPD Power-down mode, peripheral SRAM is always operating in power shut down mode and reset to default power mode after wake-up. Peripheral SRAM power mode does not change when system enters FWPD Power-down mode.

SRAM	Power-Down Mode	SRAM Power Mode Before And After Wake-Up
SRAM bank0/1/2 Key Store SRAM	PD LLPD ULLPD SPD	1.If SRAM power mode is set to normal mode, it changes to retention mode after entering Power-down Mode, and changes back to normal mode after wake-up. 2.If SRAM power mode is set to Retention or Power shut down mode, it keeps power mode setting.
	FWPD	SRAM power mode keeps power mode setting.
	DPD	SRAM power mode is always operating in power shut down mode after entering Power-down Mode, and resets to normal mode after wake-up.
Other Peripheral SRAM	PD LLPD ULLPD	1.If SRAM power mode is set to normal mode, it changes to retention mode after entering Power-down Mode, and changes back to normal mode after wake-up. 2.If SRAM power mode is set to Retention or Power shut down mode, it keeps power mode setting.
	FWPD	SRAM power mode keeps power mode setting.
	SPD	1. If SRAM power mode is set to normal mode, it changes to retention mode after entering Power-down Mode. 2. If SRAM power mode is set to Retention or Power shut down mode, it keeps power mode setting. 3. SRAM power mode is reset to default power mode after wake-up.
	DPD	SRAM power mode is always operating in power shut down mode after entering Power-down Mode, and resets to default power mode after wake-up.

Table 6.2-8 SRAM Power Mode Behavior

6.2.9 Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator, 48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, to automatically get accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL12M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL12M[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS12M[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate

within 0.25% deviation. In another case, the system needs an accurate 48 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL48M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL48M[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS48M[8] HIRC48 frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

HIRC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock are not stable or the system go into power down, HIRC trim will not be enable.

6.2.10 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These write-protected system control registers, as listed in Table 6.2-9, have write-protection after the power-on reset till user disables register protection.

Before writing to these protected registers, user has to unlock the write-protected mechanism by writing a register protection disable sequence to the REGLCTL register. The register protection disable sequence is writing the data “59h”, “16h” “88h” sequentially. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

Once a register protection disable sequence is writing to the REGLCTL register successfully, These write-protected registers will be unlocked and able to accept write access. It’s recommended to locked these registers by writing any value to REGLCTL register.

6.2.10.1 Register Lock Control mechanism with Trustzone

For M2354, due to Trustzone technology, system resources are divided into secure and non-secure, leading to type of register of peripheral is either secure or non-secure. Secure registers exist in 0x4nnn_nnnn region (i.e. bit[28] is 0), while non-secure registers exist in 0x5nnn_nnnn region (i.e. bit[28] is 1).

The security types of registers are defined by which peripheral they belong to. Secure peripheral has only secure registers while non-secure peripheral has only non-secure registers. Note that shared registers in some peripherals are also defined as non-secure registers. Refer to **SCU “Memory Access Policy”** section for more details.

There are two REGLCTL registers in system. Secure REGLCTL is SYS_REGLCTL register at address 0x40000100 for secure code to unlock write-protection of both secure and non-secure registers; Non-secure REGLCTL is SYS_REGLCTLNS register at address 0x50000100, which can be seen as the non-secure alias address of SYS_REGLCTL and is used for non-secure code to unlock write-protection of non-secure registers. Note that address listed in Table 6.2-9 is the address of secure register, for non-secure register, the first nibble of the address is 0x5.

Item	Security Type	Address
SYS_IPRST0	Secure and Non-secure	0x4000_0008
SYS_BODCTL	Secure	0x4000_0018
SYS_PORCTL	Secure	0x4000_0024
SYS_VREFCTL	Secure	0x4000_0028
SYS_USBPHY	Secure	0x4000_002C
SYS_SRAMPC0	Secure	0x4000_00DC

SYS_SRAMPC1	Secure	0x4000_00E0
SYS_PORCTL1	Secure	0x4000_01EC
SYS_PSWCTL	Secure	0x4000_01F4
SYS_PLCTL	Secure	0x4000_01F8
SYS_PLSTS	Secure	0x4000_01FC
CLK_PWRCTL	Secure	0x4000_0200
CLK_APBCLK0	Secure	0x4000_0208
CLK_CLKSEL0	Secure	0x4000_0210
CLK_CLKSEL1	Secure	0x4000_0214
CLK_PLLCTL	Secure	0x4000_0240
CLK_CLKDSTS	Secure	0x4000_0274
CLK_PMUCTL	Secure	0x4000_0290
NMIEN	Secure	0x4000_0300
AHBMCTL	Secure	0x4000_0400
FMC_ISPCTL	Secure and Non-secure	0x4000_C000
FMC_ISPTRG	Secure and Non-secure	0x4000_C010
FMC_ISPSTS	Secure and Non-secure	0x4000_C040
FMC_CYCCTL	Secure	0x4000_C04C
WDT_CTL	Secure	0x4004_0000
WDT_ALTCTL	Secure	0x4004_0004
EWDT_CTL	Secure or Non-secure	0x4004_2000
EWDT_ALTCTL	Secure or Non-secure	0x4004_2004
TIMER0_CTL	Secure	0x4005_0000
TIMER1_CTL	Secure	0x4005_0100
TIMER2_CTL	Secure or Non-secure	0x4005_1000
TIMER3_CTL	Secure or Non-secure	0x4005_1100
TIMER4_CTL	Secure or Non-secure	0x4005_2000
TIMER5_CTL	Secure or Non-secure	0x4005_2100
TIMER0_PWMCTL	Secure	0x4005_0040
TIMER1_PWMCTL	Secure	0x4005_0140
TIMER2_PWMCTL	Secure or Non-secure	0x4005_1040
TIMER3_PWMCTL	Secure or Non-secure	0x4005_1140
TIMER4_PWMCTL	Secure or Non-secure	0x4005_2040
TIMER5_PWMCTL	Secure or Non-secure	0x4005_2140

TIMER0_PWMDTCTL	Secure	0x4005_0058
TIMER1_PWMDTCTL	Secure	0x4005_0158
TIMER2_PWMDTCTL	Secure or Non-secure	0x4005_1058
TIMER3_PWMDTCTL	Secure or Non-secure	0x4005_1158
TIMER0_PWMBRKCTL	Secure	0x4005_0070
TIMER1_PWMBRKCTL	Secure	0x4005_0170
TIMER2_PWMBRKCTL	Secure or Non-secure	0x4005_1070
TIMER3_PWMBRKCTL	Secure or Non-secure	0x4005_1170
TIMER0_PWMSWBRK	Secure	0x4005_007C
TIMER1_PWMSWBRK	Secure	0x4005_017C
TIMER2_PWMSWBRK	Secure or Non-secure	0x4005_107C
TIMER3_PWMSWBRK	Secure or Non-secure	0x4005_117C
TIMER0_PWMINTSTS1	Secure	0x4005_008C
TIMER1_PWMINTSTS1	Secure	0x4005_018C
TIMER2_PWMINTSTS1	Secure or Non-secure	0x4005_108C
TIMER3_PWMINTSTS1	Secure or Non-secure	0x4005_118C
EPWM_CTL0	Secure or Non-secure	0x4005_8000/0x4005_9000
EPWM_CTL1	Secure or Non-secure	0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	Secure or Non-secure	0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	Secure or Non-secure	0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	Secure or Non-secure	0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	Secure or Non-secure	0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	Secure or Non-secure	0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	Secure or Non-secure	0x4005_80D0/0x4005_90D0
EPWM_SWBRK	Secure or Non-secure	0x4005_80DC/0x4005_90DC
EPWM_INTEN1	Secure or Non-secure	0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	Secure or Non-secure	0x4005_80EC/0x4005_90EC
BPWM_CTL0	Secure or Non-secure	0x4005_A000/0x4005_B000

Table 6.2-9 List of Registers with Write Protection

6.2.11 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm®Cortex®-M23 Technical Reference Manual*" and "*Arm®v8-M Architecture Reference Manual*".

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority.
- Interrupt tail-chaining.
- An external Non maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.13 Security Attribution Unit (SAU)

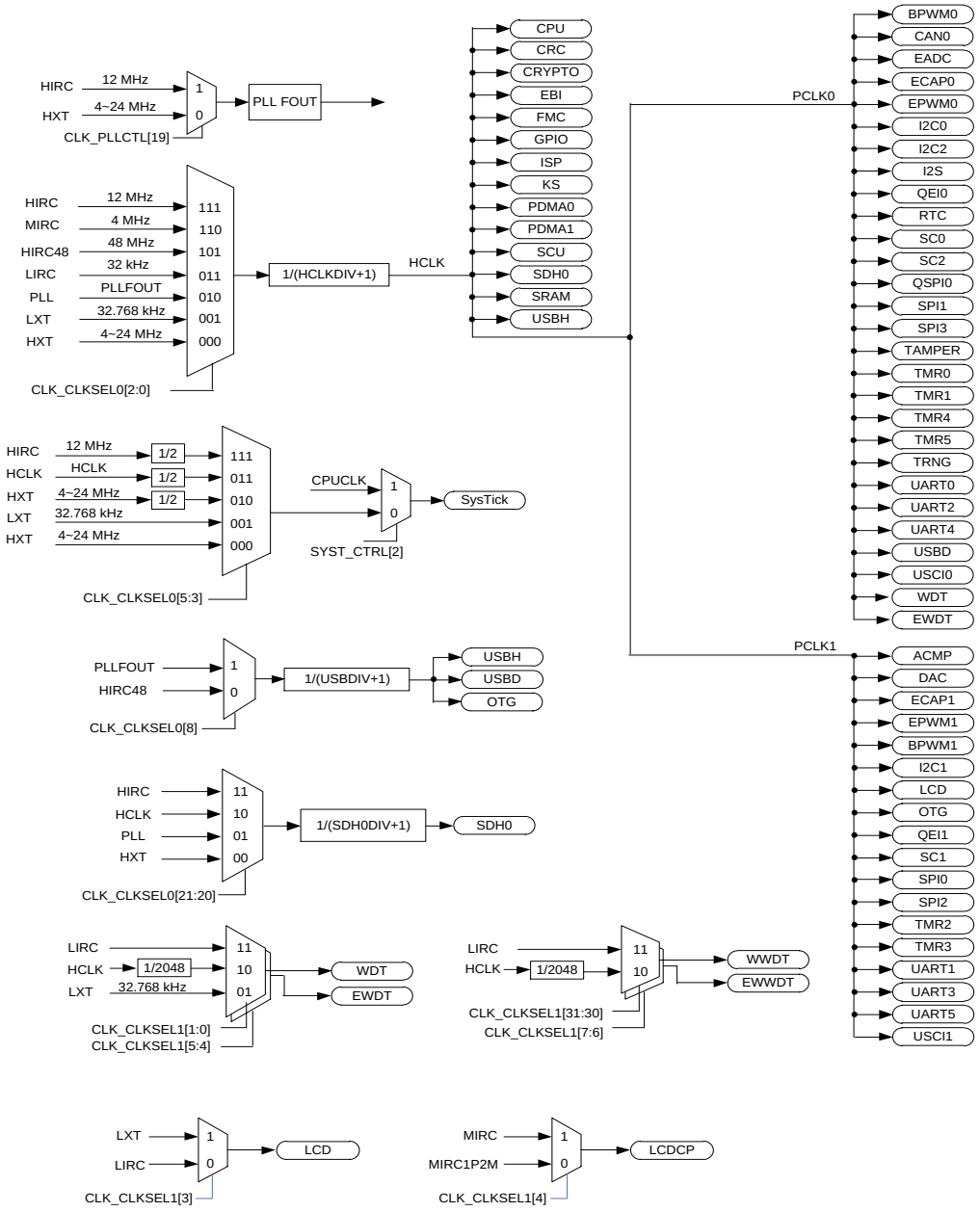
The Arm® Cortex®-M23 has an security attribution unit (SAU) to support hardware Arm® TrustZone® technique. The NuMicro® M2354 supports up to 8 memory regions in SAU for secure code to configure, and provides the memory alias architecture which can work only with proper setting of SAU, IDAU and SCU. IDAU has already defined all memory regions that should be non-secure (refer to the “Address Space Partition” section). Secure code should properly set these regions to non-secure by setting SAU. However, secure code should overwrite NSC regions to secure regions to prevent from being unexpectedly accessed by non-secure code.

SAU can be accessed by secure code. Non-secure access to all SAU registers will be RAZ/WI.

6.3 Clock Controller

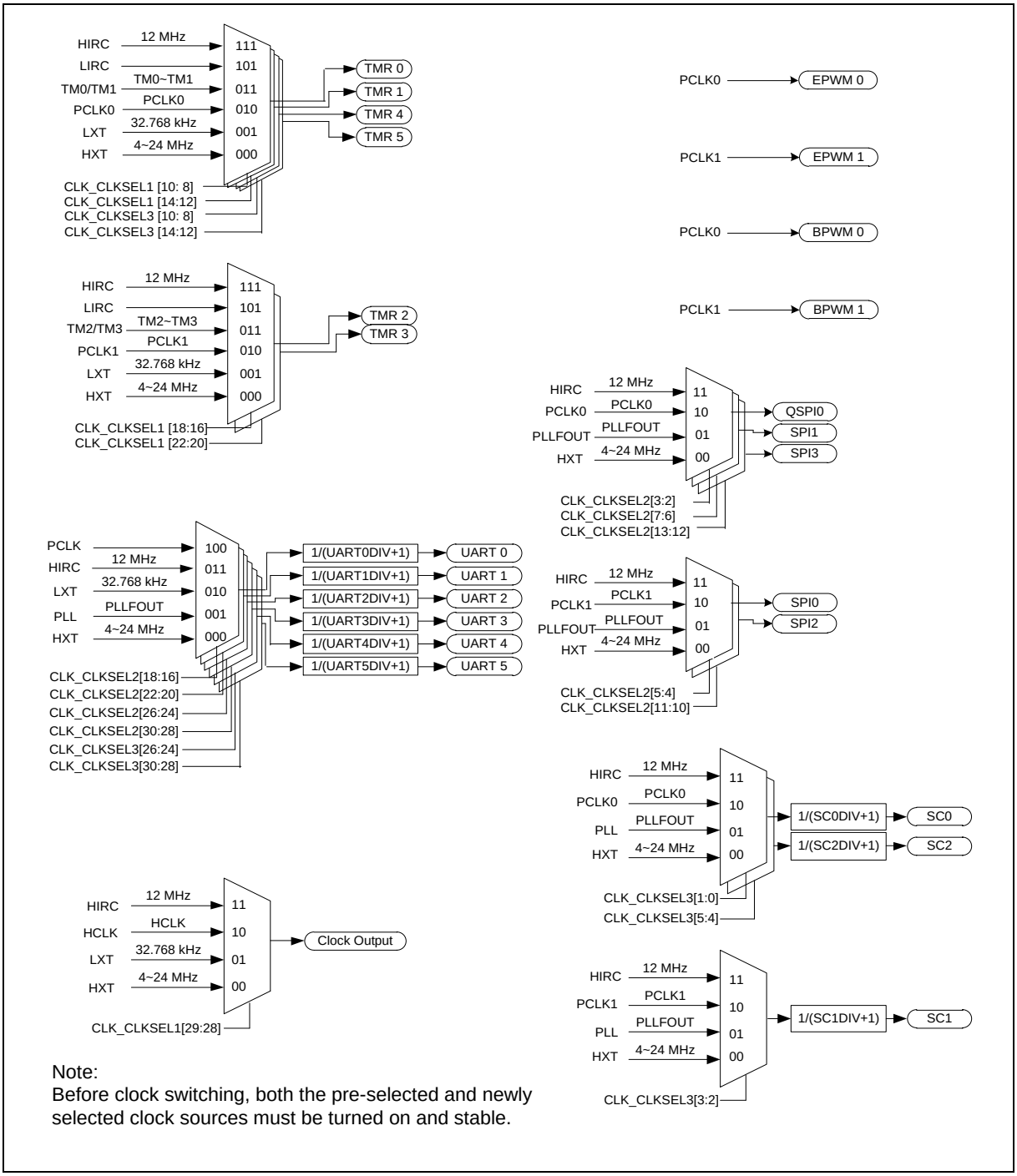
6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN (CLK_PWRCTL[7]) and core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC48), 4 MHz internal medium speed RC oscillator (MIRC) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 to Figure 6.3-3 show the clock generator and the overview of the clock source control.



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-1 Clock Generator Global View Diagram (1/3)



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-2 Clock Generator Global View Diagram (2/3)

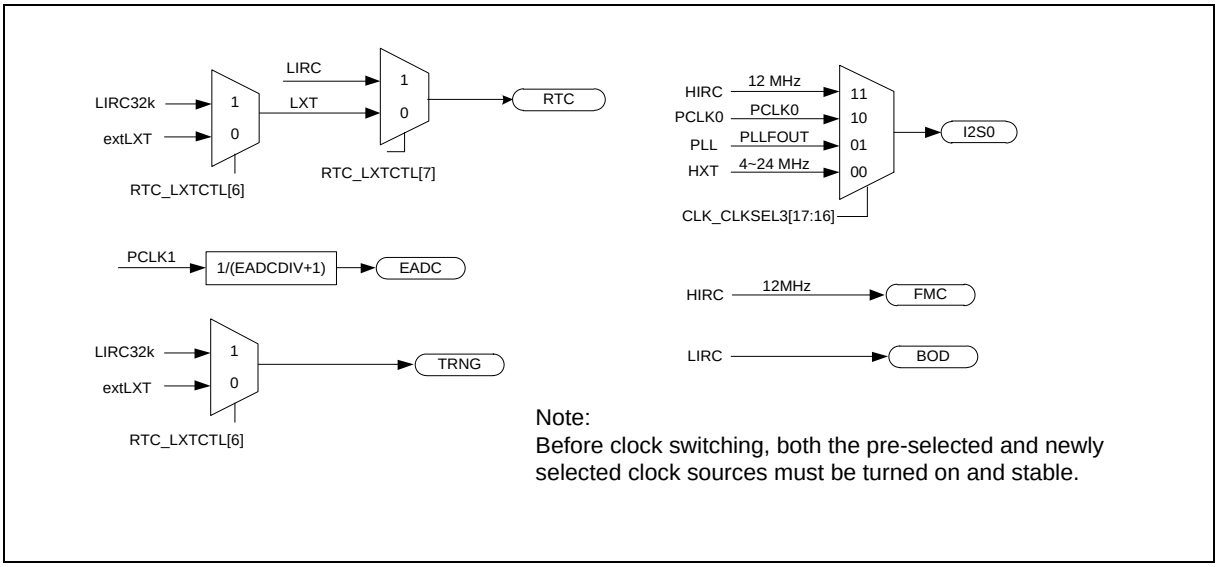
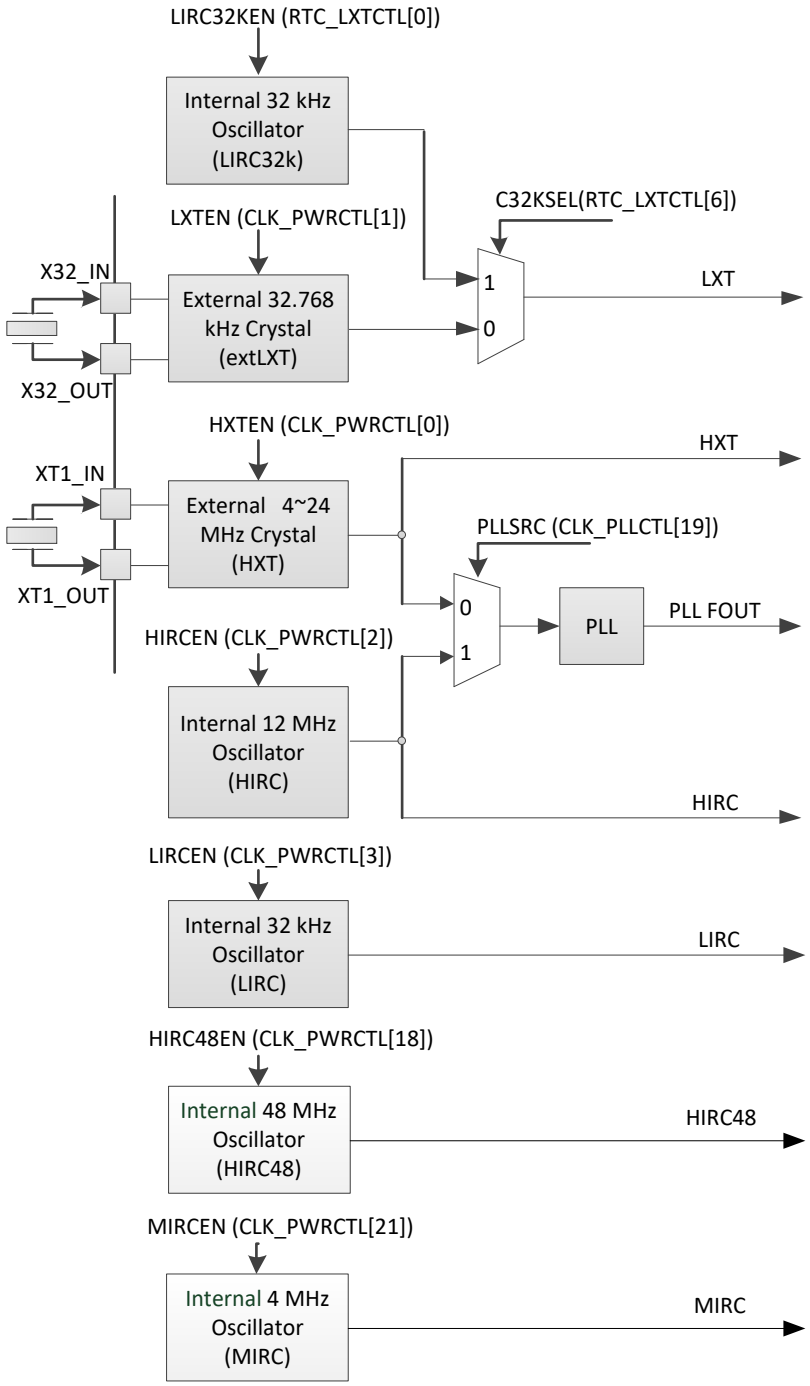


Figure 6.3-3 Clock Generator Global View Diagram (3/3)

6.3.2 Clock Generator

The clock generator consists of 7 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 4 MHz internal medium speed RC oscillator (MIRC)
- 48 MHz internal high speed RC oscillator (HIRC48)
- 32 kHz internal low speed RC oscillator (LIRC)



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-4 Clock Generator Block Diagram

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index is set to 1 after stable counter value reach a define value.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-1 will auto clear when user disables the clock source.

Besides, the clock stable index of HXT, HIRC, MIRC, HIRC48 and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
HXT	HXTEN (CLK_PWRCTL[0])	HXTSTB (CLK_STATUS[0])
LXT	LXTEN (CLK_PWRCTL[1]) or LIRC32KEN (RTC_LXTCTL[0])	LXTSTB (CLK_STATUS[1])
PLL	PD (CLK_PLLCTL[16])	PLLSTB (CLK_STATUS[2])
LIRC	LIRCEN (CLK_PWRCTL[3])	LIRCSTB (CLK_STATUS[3])
HIRC	HIRCEN (CLK_PWRCTL[2])	HIRCSTB (CLK_STATUS[4])
MIRC	MIRCEN (CLK_PWRCTL[21])	MIRCSTB (CLK_STATUS[5])
HIRC48	HIRC48EN (CLK_PWRCTL[18])	HIRC48STB (CLK_STATUS[6])
extLXT	LXTEN (CLK_PWRCTL[1])	EXTLXTSTB (CLK_STATUS[8])
LIRC32	LIRC32KEN (RTC_LXTCTL[0])	LIRC32STB (CLK_STATUS[9])

Table 6.3-1 Each Clock Source Enable Bit and Corresponding Stable Flag Table

6.3.3 System Clock and SysTick Clock

The system clock has 7 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-5.

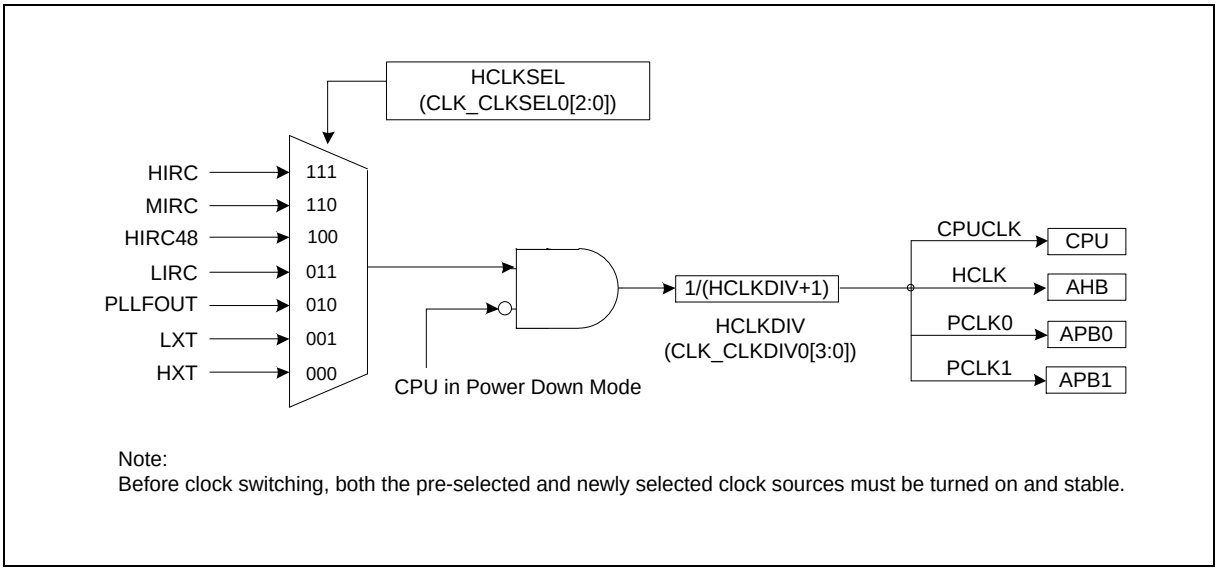


Figure 6.3-5 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

When LXT clock detector is enabled, the system clock will auto switch to LIRC if LXT clock stop being detected on the following condition: system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIE (CLK_CLKDCTL[5]) is set to 1. LXT clock source stable flag, LXTSTB (CLK_STATUS[1]), will be cleared if LXT stops when using LXT fail detector function. User can trying to recover LXT by disable LXT and enable LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recover to oscillate after re-enable action and user can switch system clock to LXT again.

The HXT clock stopping detecting and system clock switch to HIRC procedure is shown in Figure 6.3-6.

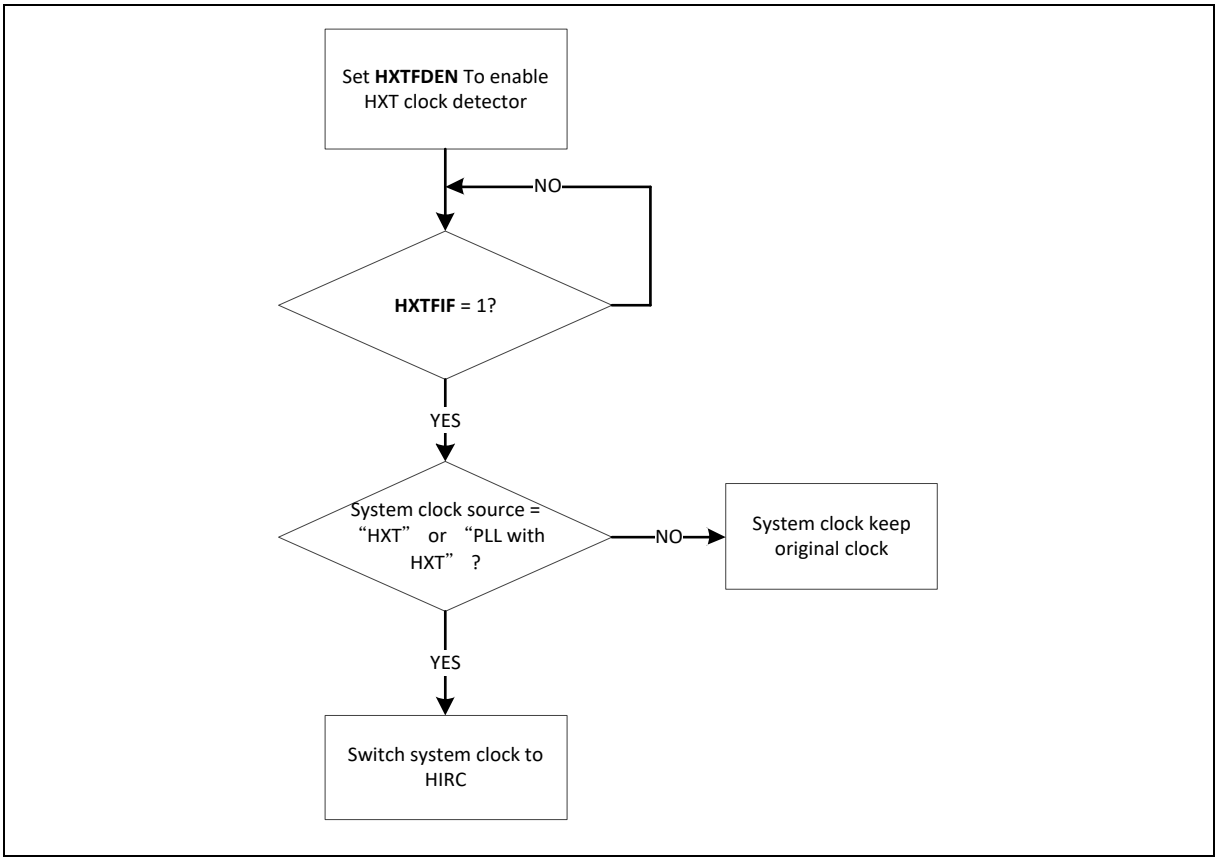
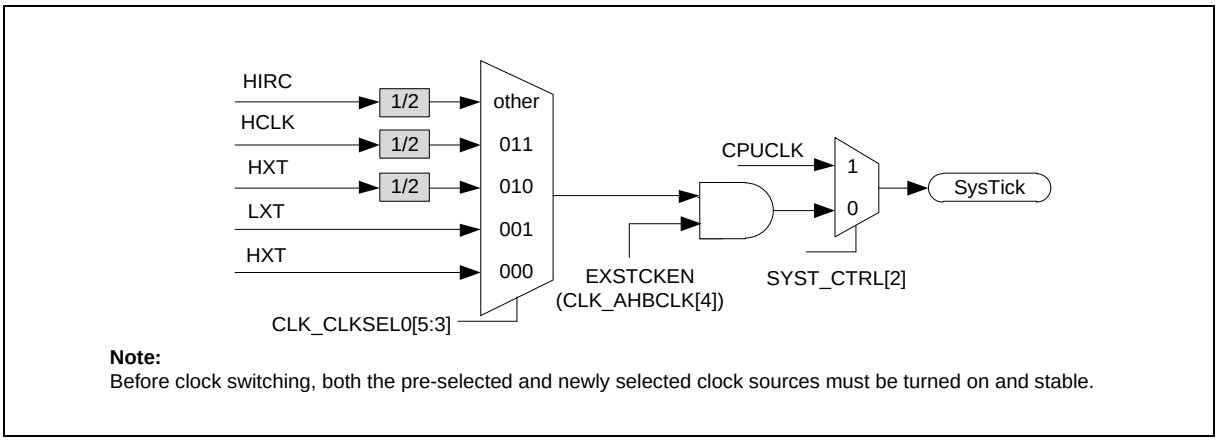


Figure 6.3-6 HXT Stop Protect Procedure



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-7 SysTick Clock Control Block Diagram

The clock source of SysTick in processor can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-7.

6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 32 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
  - 4 MHz internal medium speed RC oscillator (MIRC) clock when TIMER4~5 or LCDCP select MIRC as peripheral clock source
- Peripherals Clock
  - when the modules adopt LXT or LIRC as clock source
  - when TIMER4~5 or LCDCP select MIRC as peripheral clock source

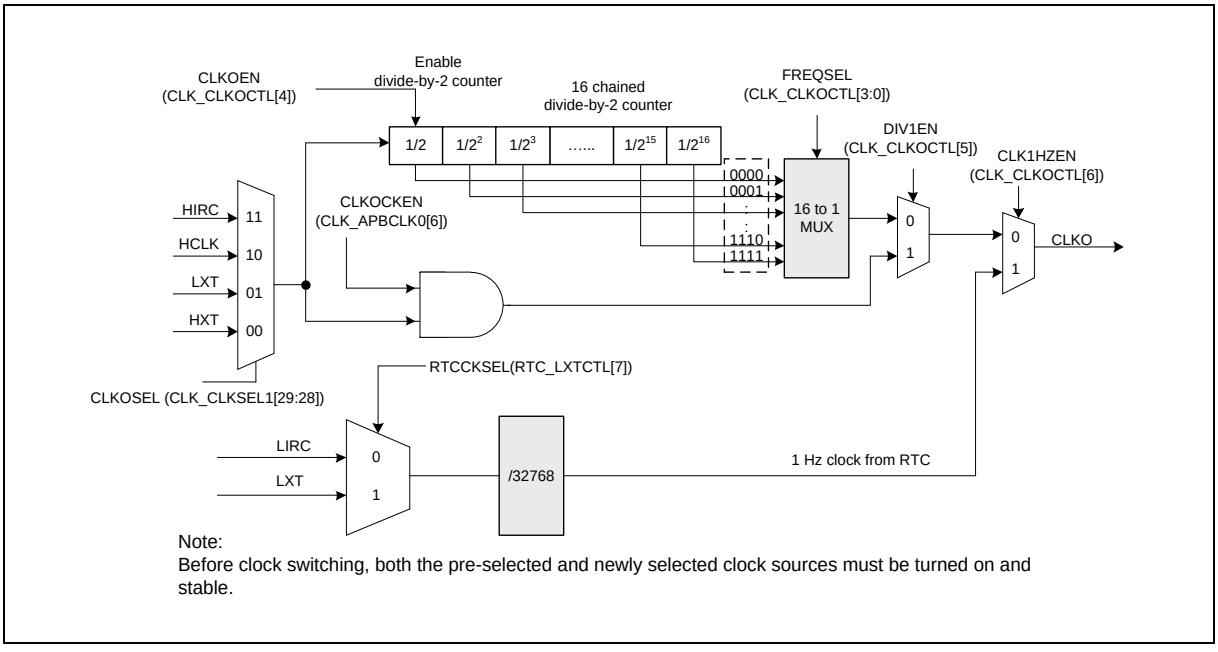
6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]). When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIV1EN(CLK_CLKOCTL[5]) is set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The output divider clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT.



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-8 Clock Output Block Diagram

6.3.7 Share Registers

The clock controller shares part of register information to non-secure world with enable bits in SYSSIAEN (SCU_SINFAEN[1]) register. Shared registers are enabled by default.

Shared Register Access	Clock Controller
R/W	NA
Read only	CLK_PWRCTL, CLK_AHBCLK, CLK_APBCLK0, CLK_APBCLK1, CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3, CLK_CLKDIV0, CLK_CLKDIV1, CLK_CLKDIV4, CLK_PLLCTL, CLK_STATUS
Write only	NA

Table 6.3-2 Clock Controller Share Register list

6.4 Security Configuration Unit (SCU)

6.4.1 Overview

Security configuration unit is designed for Arm® TrustZone®, and used to configure the security and privilege attribution of SRAM, GPIO and all other peripherals. SCU also collects AHB slaves' security and privilege violation response and generates SCU interrupt. SCU is also equipped with a timer to monitor the duration of the core processor in non-secure state.

Note: For details on Arm® TrustZone®, refer to the section "Arm® TrustZone®"

6.4.2 Features

- Configure SRAM's security and privilege attribution block by block
- Configure GPIOs' security and privilege attribution pin by pin
- Configure peripherals' security and privilege attribution
- Generate secure and privilege violation interrupt
- Equipped with a 24-bit timer as a non-secure state monitor
- Monotonic firmware version counter
- Debug protection mechanism
- Product life-cycle management

6.5 Arm® TrustZone®

The Arm® TrustZone® can be considered as a physical partition that divides the microcontroller into **Secure** (Trusted) and **Non-secure** (Non-trusted) worlds according to memory address. The secure world is an isolated execution environment, code and data loaded inside are protected and cannot be accessed from Non-secure world. Code running at secure world is called secure code that can access both secure and non-secure memories and peripherals; while code running at non-secure world is called non-secure code that can only access non-secure memories and peripherals.

Figure 6.5-1 shows an example of a system divided into the secure world and non-secure world. Green blocks indicate secure components, Red blocks indicate non-secure components and white ones are both/either secure and/or non-secure accessible. When the core processor is in secure state (left side of the figure), it belongs to secure world, which has its own MSP, PSP and VTOR registers and can access the green, red, white blocks. Contrarily, when the core processor is in non-secure state (right side of the figure), it belongs to non-secure world, which also has its own MSP, PSP and VTOR registers, but, it can only access red and white blocks so that non-secure world components are not able to impact secure world.

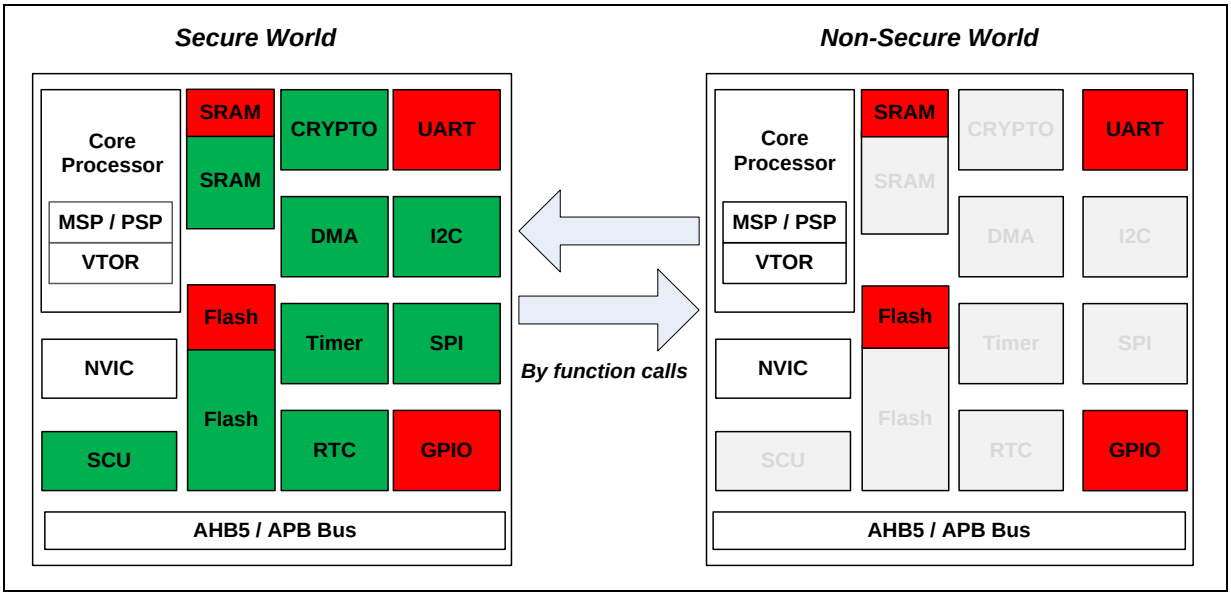


Figure 6.5-1 Secure World View and Non-secure World View on a Chip

In order to support TrustZone® to set up both secure world and non-secure world, Cortex®-M23 provides three security attributes. Each memory address is assigned with one of the security attributes. These security attributes are listed below.

- Non-secure (NS)

  Addresses used for non-secure memory or non-secure peripheral's registers.

- Secure (S)

  Addresses used for secure memory or secure peripheral's registers.

- Non-secure Callable (NSC)

  A special type of secure memory region which can contain SG instructions. The SG instruction allows a non-secure function calls to a secure function.

The address space partitioning is completed by Implementation Define Attribution Unit (IDAU) and Security Attribution Unit (SAU) together. The IDAU is non-programmable, which defines static partition

of address space. The static partition specifies the default security attribute of a memory region. In contrast with IDAU, the SAU is programmable which provides dynamic partition of address space. The dynamic partition is given by software programmer to specify the security attribute of a memory region. The core processor is in secure state when executing instructions from secure memory. Otherwise, the core processor is in non-secure state when executing instructions from non-secure memory. For setting IDAU and SAU, refer to sections “Implementation Defined Attribution Unit (IDAU)” and “Security Attribution Unit (SAU)” in “System Manager” chapter for more details.

The security attribute of Flash, SRAM and peripherals are assigned by TrustZone® related control units. The NSCBA register in FMC is used to divide the APROM into two parts, one is secure and the other is non-secure. The security attribute of SRAM and peripherals are assigned by programming Secure Configuration Unit (SCU).

Whenever being reset, the M2354 is in secure state, that is, the core processor, Flash, SRAM and peripherals are all in secure state. Therefore, the system boots in secure state. The boot code is responsible to set up TrustZone® related control units in M2354 to partition address space and assign non-secure resources that can be directly accessed from non-secure world.

6.5.1 Address Space Partition

The SAU and IDAU are the control units used to define security attribute of memory addresses. The IDAU defines default partition of secure and non-secure addresses, while the SAU is programmable to change the security attribute defined by IDAU.

6.5.1.1 Implementation Define Attribution Unit (IDAU)

The IDAU uses address bit 28 to distinguish between secure and non-secure world, i.e. the bit 28 of a secure address is always 0, and the bit 28 of a non-secure address is always 1, except regions above 0xE000_0000.

The partition of 4GB address space is shown as Figure 6.5-2. Each region consists of a secure (bit 28 is 0) and a non-secure (bit 28 is 1) sub-regions, the size of a sub-region is 256 Mbytes. In order to store entry functions for non-secure code, the security attribute of secure SRAM region is assigned as non-secure callable (**NSC**). Similarly, the secure “Code” region is assigned as NSC but has an exception at first 2 KB area. This first 2 KB area is defined as secure only to avoid accidental **SG** instruction after power on.

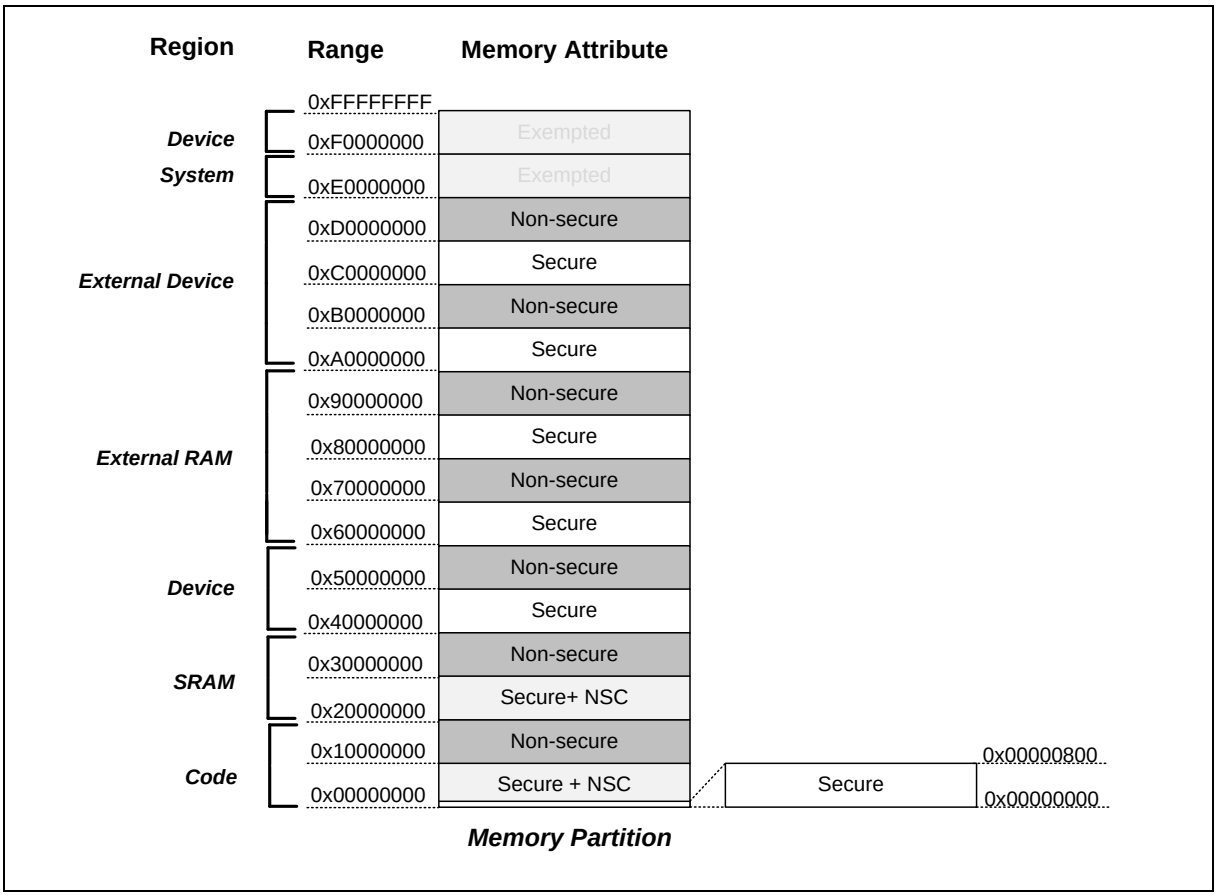


Figure 6.5-2 The 4 GB Memory Map Divided Into Secure and Non-secure Regions by IDAU

6.5.1.2 Security Attribution Unit (SAU)

The SAU is a MPU-like function unit inside Cortex®-M23. Up to 8 memory regions can be defined by programming control registers of SAU.

Memory regions are enabled individually by programming SAU_RNR, SAU_RBAR and SAU_RLAR. The memory region is enabled once RENABLE (SAU_RLAR[0]) is set to 1, and the security attribute is defined by NSC (SAU_RLAR[1]):

- NSC = 0, the memory region is Non-secure (NS).
- NSC = 1, the memory region is Secure and Non-secure callable (NSC).

The security attribute of each memory region defined by SAU is either NS or NSC. Those memory addresses not defined by SAU regions are treated as Secure. After all memory regions are set, SAU_CTRL[0] should be set to 1 to enable SAU.

Both IDAU and SAU define the security attribute of a memory address. If the definitions are different, the more secure attribute will be used for the memory address. The priority of the security attribute from high to low is Secure > NSC > NS.

When the core processor attempts to access a target, e.g. a memory or peripheral register, the security attribute of the target is decided by checking IDAU and SAU. If the core processor is non-secure but the target is secure, a HardFault exception will be generated. Because non-specified memory addresses are treated as secure, non-secure memory regions need to be defined for the core processor to access

non-secure memory and non-secure peripheral registers. Besides, whole secure code and SRAM regions are defined as NSC by IDAU. The size of NSC regions can be changed according to the NSC entry functions included in application code. The example usage of SAU regions is shown as Figure 6.5-3.

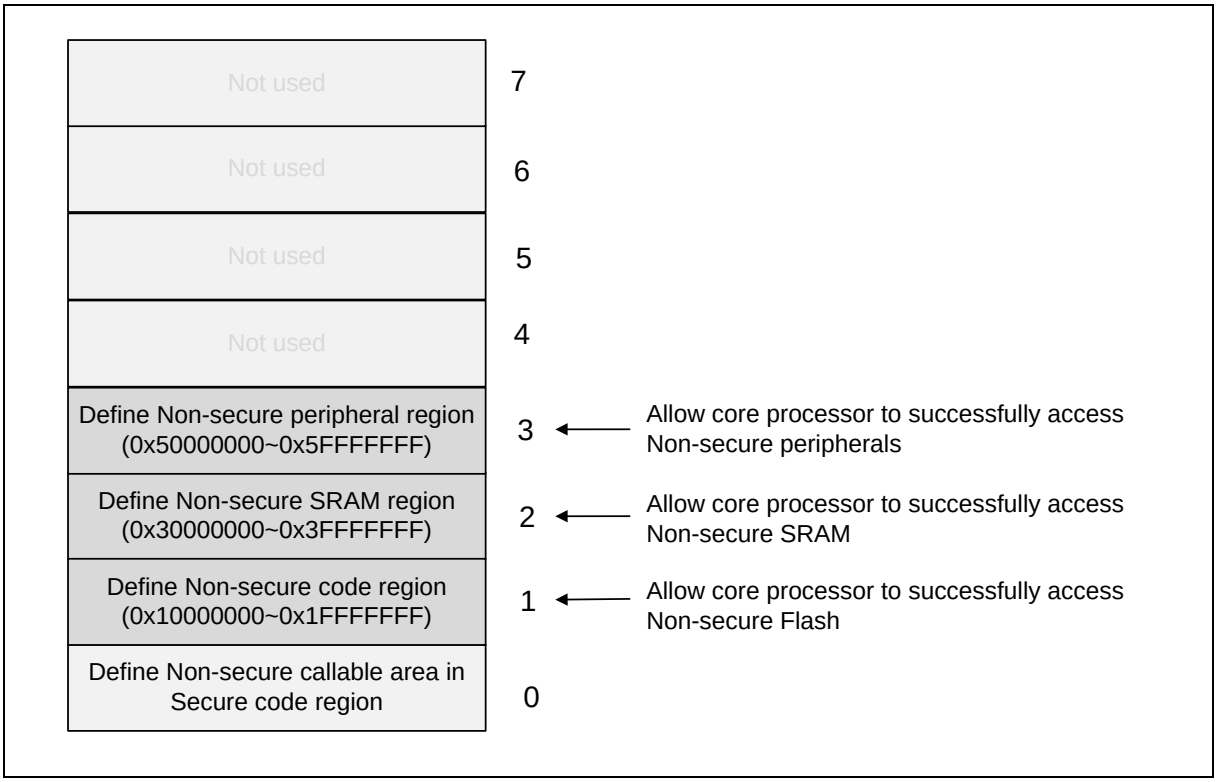


Figure 6.5-3 Typical Setting of SAU

6.5.2 Security Attribute Configuration

The previous section describes how to divide the address space of core processor view into secure world and non-secure world. For M2354, the memory and peripherals can be assigned to either secure or non-secure world during system initialization. The M2354 is designed to start execution in secure state after reset. In other words, core processor and all system resources including Flash, SRAM and peripherals are secure after reset. Then, the system initialization code may change some parts of the system resources to be non-secure.

6.5.2.1 Security Attribute Configuration of Flash

The M2354 Flash memory is split into a number of different regions such as LDROM, APROM and others. Most of the Flash regions are always secure and cannot be changed. The only one can be changed is the APROM region. Non-secure APROM region is set by programming a special control register, NSCBA (Non-secure base address). The NSCBA[23:0] indicates the starting address of non-secure APROM and its value should be aligned with a Flash page size. The secure APROM region starts from address 0x0 and ends at NSCBA[23:0] – 1, while the non-secure APROM region ranges from NSCBA[23:0] to the end of APROM. For setting NSCBA, refer to FMC section for more details.

6.5.2.2 Security Attribute Configuration of SRAM and Peripherals

The secure state of SRAM blocks and all peripherals can be configured by Security Configuration Unit (SCU), which contains a set of control registers used to assign the security attribute. Besides, the SCU monitors bus transfers to detect unsecure access. The unsecure access is one of the following conditions.

- Non-secure master peripheral tries to access a secure address (address bit 28 = 0).
- Secure code or secure master peripheral uses non-secure address (address bit 28 = 1) to access secure SRAM or peripheral.

When an unsecure access is detected, SCU blocks the access operation and generates a secure alarm interrupt.

For more details, refer to the Security Configuration Unit (SCU) chapter.

6.5.3 System Address Map and Access Scheme

In the M2354 series, the Flash, SRAM and most peripherals can be assigned to be Secure or Non-secure, but each of them can be accessed through either Secure address or Non-secure address depending on its security attribute configuration. Core processor and master peripherals should use correct address to access resources, i.e. the secure resource should be accessed by using secure address. Similarly, the non-secure resource should be accessed by using non-secure address.

6.5.3.1 Permanent Secure Peripherals

The security attribute of some peripherals are always secure and cannot be changed for safety and security. If necessary, the secure code should manage and provide functions for non-secure code to access these peripherals. Table 6.5-1 lists these secure peripherals.

Peripheral	Function	Address
SYS	System Control Registers	0x4000_0000 – 0x4000_01FF
CLK	Clock Control Registers	0x4000_0200 – 0x4000_02FF
NMI	NMI Control Registers	0x4000_0300 – 0x4000_03FF
PDMA0	Peripheral DMA 0 Control Registers	0x4000_8000 – 0x4000_8FFF
FMC	Flash Memory Control Registers	0x4000_C000 – 0x4000_CFFF
SCU	Security Configuration Unit Registers	0x4002_F000 – 0x4002_FFFF
WDT	Watchdog Timer Control Registers	0x4004_0000 – 0x4004_0FFF
TMR01	Timer0/Timer1 Control Registers	0x4005_0000 – 0x4005_0FFF

Table 6.5-1 Peripherals and Regions that are Always Secure

6.5.3.2 Secure Address vs. Non-secure Address

A memory or a peripheral register may have secure and non-secure address in system address map, but the memory or register only responds to the address that is consistent with its security attribute. The different access modes of secure and non-secure target are illustrated in Figure 6.5-4.

Suppose that SRAM block 0, 2, and 4 are in secure state, they will respond to an access when address bit 28 is 0 (secure address), but will not respond to an access with address bit 28 is 1 (non-secure address). In this example, SRAM block 1 and 3 are in non-secure state. Hence, these blocks will only respond to an access when the address bit 28 is 1.

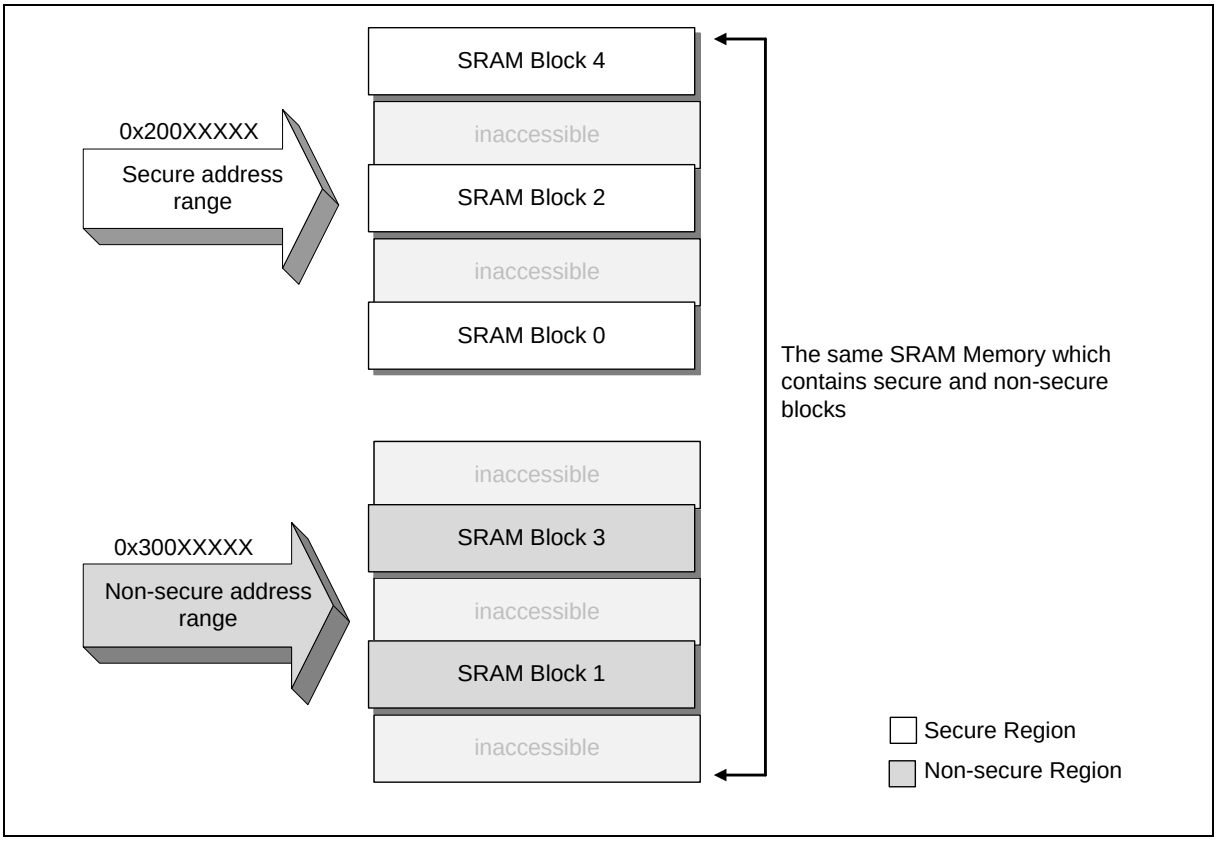


Figure 6.5-4 Example of SRAM Divided Into Secure Block and Non-secure Block

6.5.3.3 Valid Access vs. Invalid Access

When core processor or a master peripheral is trying to access (read or write) a memory or register, the result depends on the following conditions.

- Non-secure code or master peripheral is not allowed to access a secure memory or register.
- A memory or register only responds to the related address which is consistent with its security attribute.

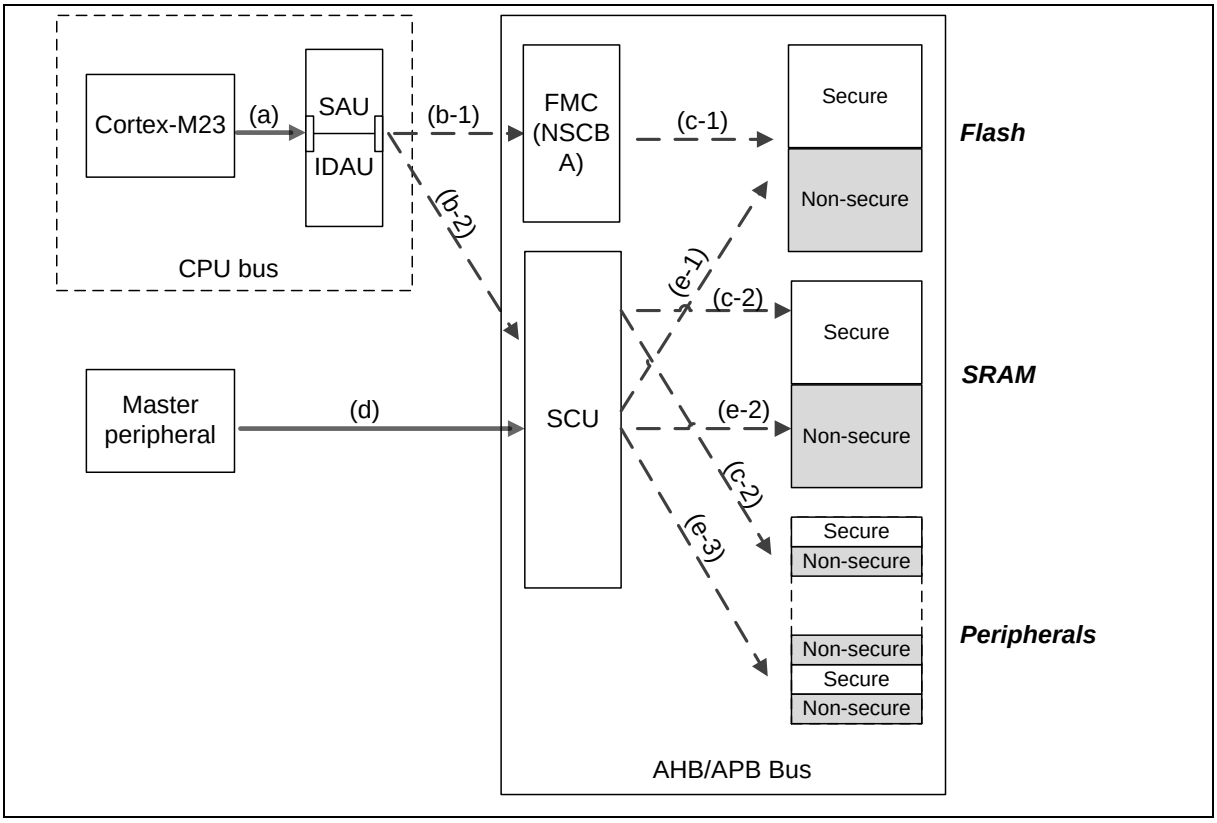


Figure 6.5-5 Checking Point of Accesses

Figure 6.5-5 illustrates how the above conditions are checked by TrustZone® related control units.

When the core processor tries to fetch instructions or access data, the security attribute of the core processor and target address are verified by SAU and IDAU (refer to (a)). If the core processor is in non-secure state and target address is secure, a hard fault exception will be generated. The other cases will go to next checkpoints (refer to (b-1) and (b-2)). If the non-secure code tries to read/write a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure code uses non-secure address to access a secure memory or register, the operation has no effect. (refer to (c-1) and (c-2))

When a master peripheral tries to read/write a memory or register, the SCU will verify the access (refer to (d)). When a non-secure master peripheral wants to access a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure master peripheral uses non-secure address to read/write a secure memory or register, the operation has no effect.

The responses of the accesses from the core processor and master peripherals follow the rule called memory access policy, which is described in the “Memory Access Policy (MAP)” section of “Security Configuration Unit (SCU)” chapter.

6.6 Flash Memory Controller (FMC)

6.6.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application. Both BANK0 and BANK1 have 256/512 Kbytes space. Thus, the total size of application rom (APROM) is 512K/1024K. A User Configuration block provides for system initiation in BANK0. A 16 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function in BANK0. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data in BANK1. A 16K Secure Bootloader is used to check boot code integrity and authenticity, and consists of native ISP functions. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.6.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports dual-bank remapping
- Supports 512/1024 Kbytes application ROM (APROM)
- Supports 16 Kbytes loader ROM (LDROM)
- Supports 4 XOM (Execution Only Memory) regions to conceal user program in APROM.
- Supports 8K Data Flash
- Supports 16 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 2 Kbytes page erase for all embedded Flash
- Supports bank erase for APROM, except XOM regions.
- Supports two level locks for protecting secure region and non-sec region.
- Supports Secure Bootloader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for check boot code integrity and authenticity
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports Non-Secure In-System-Programming (NS ISP) to update embedded Non-Secure Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

6.7 General Purpose I/O (GPIO)

6.7.1 Overview

This chip has up to 106 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 106 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB and PE has 16 pins on port. PC and PD has 14 pins on port. PF has 12 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of the 107 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Please refer to the M2354 Datasheet for detailed pin operation voltage information about V_{DD}, V_{DDIO} and V_{BAT} electrical characteristics. PA10, PA11, PA13~15, PB0~15, PF2, PF3 are not support 5V tolerance.

6.7.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function
- Improve access efficiency by using single cycle I/O bus

6.8 PDMA Controller (PDMA)

6.8.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. There are two PDMA controller PDMA0 and PDMA1. PDMA0 is secure PDMA, PDMA1 can be configured as secure or non-secure PDMA. Each PDMA controller has a total of 8 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.8.2 Features

- Supports 8 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports 2 PDMA controller PDMA0 and PDMA1, PDMA0 is secure PDMA, PDMA1 can be configured as secure or non-secure PDMA
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and USB, UART, USCI, SPI, EPWM, I^2C, I^2S, Timer, ADC, and DAC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5
- Supports enhanced stride function on channel 0 and channel1

6.9 Timer Controller (TMR)

6.9.1 Overview

The timer controller includes six 32-bit timers, Timer0 ~ Timer5, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides the PWM generator function. In Timer0 ~ Timer3, each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be controlled by pin mask, polarity and break control, and dead-time generator. In Timer4 and Timer5, each PWM generator supports only one PWM output channel. The output state of PWM output pin can be controlled by polarity control, output enable control and output channel select.

6.9.2 Features

6.9.2.1 Timer Function Features

- Six sets of 32-bit timers, Timer0 ~ Timer5, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture event for interval measurement
- Supports capture event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event in Timer0 ~ Timer3
- Supports internal clock (HIRC, LIRC, MIRC) and external clock (HXT, LXT) for capture event in Timer4 and Timer5
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, EADC, DAC and PDMA function
- Supports Timer4 and Timer5 time-out interrupt signal or capture interrupt signal to trigger EADC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

6.9.2.2 PWM Function Features

In the Timer0 ~ Timer3 PWM,

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel

  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

In the Timer4 and Timer5 PWM,

- Supports independent mode for PWM generator with one output channel
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channel
- Supports interrupt on the following events:
  - PWM period point, up-count compared point events
- Supports wake-up when interrupt occurs when clock source is LXT, LIRC or MIRC
- PWM can generator output in Power-down mode
- Supports trigger EADC and PDMA on the following events:
  - PWM period point and up-count compared point events

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.10.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK = 32 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC 32kHz or LXT.

6.11 Extra Watchdog Timer (EWDT)

6.11.1 Overview

The Extra Watchdog Timer (EWDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.11.2 Features

- 20-bit free running up counter for EWDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.5 ms ~ 32.768 s if EWDT_CLK = 32 kHz.
- System kept in reset state for a period of (1 / EWDT_CLK) * 63
- Supports selectable EWDT reset delay period, including 1026, 130, 18 or 3 EWDT_CLK reset delay period
- Supports EWDT time-out wake-up function only if EWDT clock source is selected as LIRC 32kHz or LXT.

6.12 Window Watchdog Timer (WWDT)

6.12.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.12.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.13 Extra Window Watchdog Timer (EWWDT)

6.13.1 Overview

The Extra Window Watchdog Timer (EWWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.13.2 Features

- 6-bit down counter value (CNTDAT, EWWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, EWWDT_CTL[21:16]) to make the EWWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, EWWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of EWWDT counter
- EWWDT counter suspends in Idle/Power-down mode

6.14 Real Time Clock (RTC)

6.14.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.14.2 Features

- Supports external power pin V_{BAT}.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up 3 pairs dynamic loop tamper pin or 6 individual tamper pin.
- Built-in LXT frequency monitor.
- Supports 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports Flash mass erase operate will also clear the 80 bytes spare registers content.

6.15 EPWM Generator and Capture Timer (EPWM)

6.15.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events are used to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have different architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.15.2 Features

6.15.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared

- Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter match free trigger comparator compared value (only for EADC)
  - Supports EPWM trigger EADC event prescaler feature
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect Function.

6.15.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.16 Basic PWM Generator and Capture Timer (BPWM)

6.16.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.16.2 Features

6.16.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.16.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.17 Quadrature Encoder Interface (QEI)

6.17.1 Overview

There are two Quadrature Encoder Interfaces (QEI) controllers in this device. The QEI decodes speed of rotation and motion sensor information and can be used in any application that uses a quadrature encoder for feedback.

6.17.2 Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must be lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must be lower than Noise Filter Clk/8

6.18 Enhanced Input Capture Timer (ECAP)

6.18.1 Overview

This device provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.18.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.19 UART Interface Controller (UART)

6.19.1 Overview

The chip provides six channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

6.19.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 /UART1 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

- Support Single-wire function mode.

UART Feature	UART0/ UART1	UART2/UART3/ UART4/ UART5	SC_UART	USCI-UART
FIFO	16 Bytes	16 Bytes	4 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	-	√
IrDA	√	√	-	-
LIN	√	-	-	-
RS-485 Function Mode	√	√	-	√
nCTS Wake-up	√	√	-	√
Incoming Data Wake-up	√	√	-	√
Received Data FIFO reached threshold Wake-up	√	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-	-
Auto-Baud Rate Measurement	√	√	-	√
STOP Bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√	√
Stick Bit	√	√	-	-
Note: √= Supported				

Table 6.19-1 NuMicro® M2354 Series UART Features

6.20 Smart Card Host Interface (SC)

6.20.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.20.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.21 I²S Controller (I²S)

6.21.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.21.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.22 Serial Peripheral Interface (SPI)

6.22.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M2354 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.22.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.23 Quad Serial Peripheral Interface (QSPI)

6.23.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M2354 series contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O transfer mode and the controller supports the PDMA function to access the data buffer.

6.23.2 Features

- Supports Master or Slave mode operation
- Supports 2-bit transfer mode
- Supports Dual and Quad I/O transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.24 USCI - Universal Serial Control Interface Controller (USCI)

6.24.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.24.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.25 I²C Serial Interface Controller (I²C)

6.25.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are three sets of I²C controllers which support Power-down wake-up function.

6.25.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function.

6.26 USCI – UART Mode

6.26.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.26.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Supports 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.27 USCI - SPI Mode

6.27.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both Master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as Master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or Master device. The application block diagrams in Master and Slave mode are shown below.

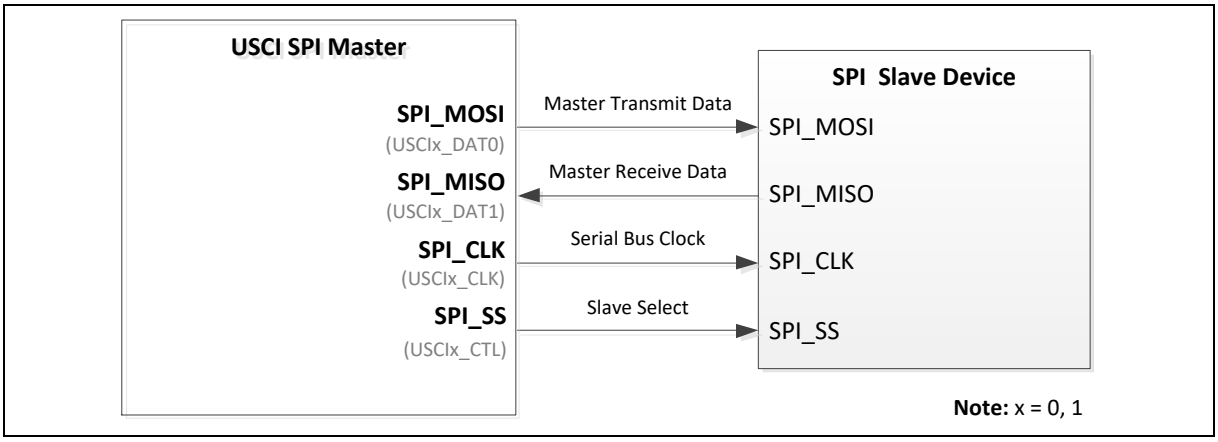


Figure 6.27-1 SPI Master Mode Application Block Diagram

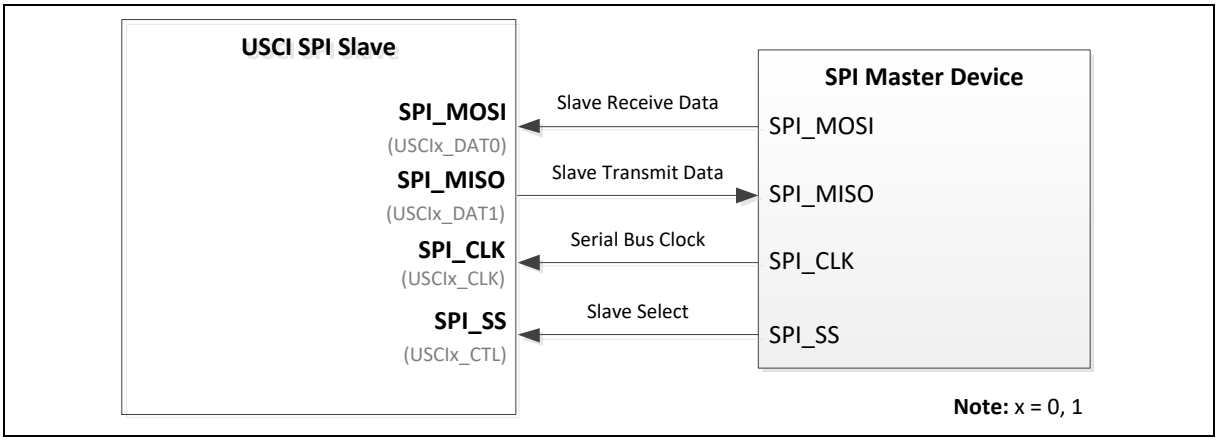


Figure 6.27-2 SPI Slave Mode Application Block Diagram

6.27.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload

- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.28 USCI - I²C Mode

6.28.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.28-1 for more detailed I²C BUS Timing.

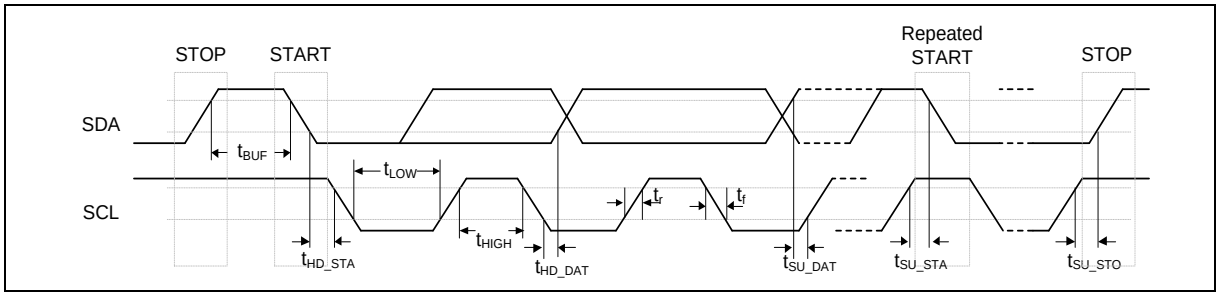


Figure 6.28-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.28.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by received 'START' symbol or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.29 Controller Area Network (CAN)

6.29.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 Mbytesit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.29.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.30 Secure Digital Host Controller (SDH)

6.30.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SD host controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.30.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.31 External Bus Interface (EBI)

6.31.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.31.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplexe mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.32 USB 1.1 Device Controller (USBD)

6.32.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK and OUT ACK, etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.32.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbytes buffer size
- Provides remote wake-up capability

6.33 USB 1.1 Host Controller (USBH)

6.33.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.33.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.34 USB On-The-Go (OTG)

6.34.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID dependent mode, USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

6.34.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

6.35 CRC Controller (CRC)

6.35.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.35.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.36 Cryptographic Accelerator (CRYPTO)

6.36.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA/HMAC, RSA, and ECC algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation. (283~571 bits are only generated for Key Store.)

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, CBC-CS3, CCM and GCM mode.

The SHA accelerator is an implementation fully compliant with the SM3, SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and corresponding HMAC (Keyed-Hash Message Authentication Code) algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with RSA cryptography, CRT decryption algorithm and side-channel attack countermeasures algorithm.

The Crypto can get key from key store and/or put key to key store determined by the function of each accelerator.

6.36.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits only generated for Key Store)
  - Able to take the true random number seed from TRNG
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports CCM mode, GCM mode and GHASH function
  - Supports SM4 block cipher algorithm
  - Supports key expander
  - Supports one technique to improve side-channel attack protection ability
- SHA
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512
  - Supports SM3 Cryptographic Hash Algorithm
- ECC
  - Supports both prime field GF(p) and binary filed GF(2^m)

- Supports NIST P-192, P-224, P-256, P-384, and P-521
- Supports NIST B-163, B-233, B-283, B-409, and B-571
- Supports NIST K-163, K-233, K-283, K-409, and K-571
- Supports Curve25519
- Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
- Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m)
- Supports modulus division, multiplication, addition and subtraction operations in GF(p)
- Supports three techniques to improve side-channel attack protection ability

- RSA
  - Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits
  - Supports CRT decryption with 2048, 3072 and 4096 bits
  - Supports three techniques to improve side-channel attack protection ability

6.37 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.37.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 16 external input channels and 3 internal channels. The ADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, Timer0~5 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.37.2 Features

- Analog input voltage range: 0~V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum ADC clock frequency is 80 MHz
- Up to 5.71 MSPS conversion rate
- Configurable ADC internal sampling time.
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
- Supports calibration and load calibration words capability.
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules:
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~15 and trigger source
  - Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power (V_{BAT})
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- An ADC conversion can be started by:
  - Write 1 to SWTRG (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~5 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers

  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.38 True Random Number Generator (TRNG)

6.38.1 Overview

The purpose of True Random Number Generator (TRNG) is to generate the randomness by extracting from physical phenomena.

6.38.2 Features

- 800 random bits per second
- Provides the true random number seed for PRNG

6.39 Key Store (KS)

6.39.1 Overview

The Key Store (KS) is the key management device and has a 4 Kbytes SRAM, 2 Kbytes Flash and OTP for key storage. The Key Store is capable of providing a crypto engine to access or storing the key while encryption, decryption and generation. The Key Store supports revoke key operation if the key is unused. The Key Store is able to protect the key by data scrambling, data remanence prevention and silent access.

6.39.2 Features

- Supports programming interface for key management
- Supports multiple key size
- Supports 4 Kbytes SRAM, 2 Kbytes Flash and 544bytes OTP for key storage
- Supports 32 keys for SRAM, 32 keys for Flash and 8 keys for OTP at most
- Supports crypto engine access or store key in key store directly
- Supports ECDH operation with ECC and PRNG engine
- Supports to store middle data for RSA CRT and SCAP mode
- Supports revoke operation for each key
- Supports erase key in SRAM/Flash and revoke key in OTP while tamper detected
- Supports integrity checking
- Supports data scrambling at SRAM, Flash and OTP
- Supports data remanence prevention at SRAM
- Supports silent access for side-channel protection at SRAM, Flash and OTP

6.40 LCD Controller

6.40.1 Overview

The LCD controller controls the device's built-in voltage/current drivers, which can drive externally connected LCD panels with up to 8 common planes (or called common electrodes, COMs) and 44 segments (SEGs). Every COM or SEG output pin of the device can supply the necessary voltage waveform to the connected LCD panels.

The LCD controller provides several configuration registers, by which users can effectively control a variety of LCD panels with specific considerations for display modes, driving capability, and power consumption.

6.40.2 Features

- Supports the following maximum COM/SEG combinations:
  - 320 pixels (8-COM x 40-SEG)
  - 252 pixels (6-COM x 42-SEG)
  - 176 pixels (4-COM x 44-SEG)
  - 104 pixels (8-COM x 13-SEG) for 64-pin package
- Supports up to 8 COM output pins, multiplexed with GPIO pins
- Supports up to 44 SEG output pins, multiplexed with GPIO pins
- Supports 3 bias levels: 1/2, 1/3, and 1/4
- Supports 8 duty ratios: 1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, and 1/8
- Supports both types A and B waveforms
- Supports a clock frequency divider, programmable from 0 to 1023, to generate the LCD operating frequency (F_{LCD})
- Supports LCD operating voltage (V_{LCD}) from 2.6 V to 3.6 V
- Selectable LCD operating voltage sources:
  - V_{LCD} (External dedicated V_{DD} pin for LCD) power
  - AV_{DD} (Analog V_{DD}) power
  - Built-in charge pump
- A built-in resistive network to generate required bias voltages
  - supports 2 drive modes: low-drive and high-drive modes
  - supports voltage buffers which are active only in the low-drive mode
- Supports a configurable power-saving mode. During this mode,
  - the resistive network temporarily changes to the low-drive mode, or
  - the voltage buffers are temporarily turned off.
- At the end of every frame, a dedicated flag is set and an interrupt can be programmed to occur.
- Supports a frame counter. At the end of frame counting, a dedicated flag is set and an interrupt can be programmed to occur.
- Supports LCD blinking capability. By using the frame counter, users have more flexibility to

adjust the blinking frequency.

- The LCD clock source is LIRC or LXT. LCD display or blinking can keep working even when the chip is in the power-down modes, only if at least one of LIRC and LXT is active.
- Supports a charging timer for the charge pump. By using this timer, users can estimate the loading of the charge pump, and adjust, if necessary, its charging power.

6.41 Tamper Controller (TC)

6.41.1 Overview

To protect the content of the Internal secrets from being attacked by hackers, the Tamper controller provides various attack detection and attack event response. The attack detection includes pins, clock and system voltage. When an attack is detected, the sensitive data like crypto session keys can be cleared by the attack event response.

6.41.2 Features

- Includes voltage, clock and I/O tamper detectors:
  - Voltage detector: detects voltage glitch including low voltage domain (LV) and high voltage domain (HV).
    - HV detector detects if V_{DD} > 4.0V
    - LV detector detects if LDO_CAP > ± 20%
    - Power loss detector indicates power status of VBAT
  - Clock detector: detects if external clock (LXT) is failed or stopped
  - I/O tamper detector: detects GPF6~11 pins
- Active shield in SRAM with power/GND and tamper I/O.
- Provides event response after an attack detected:
  - Clear key or data content in SRAM and Flash of Key Store, and revoke the OTP in Key Store
  - Clear RTC spare register
  - Reset Crypto
  - Chip reset
  - Interrupt
  - Wake up the system
- Not supported in Deep Power-down mode.

6.42 Digital to Analog Converter (DAC)

6.42.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12-or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.42.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 12-or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

6.43 Analog Comparator Controller (ACMP)

6.43.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.43.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagaion speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode

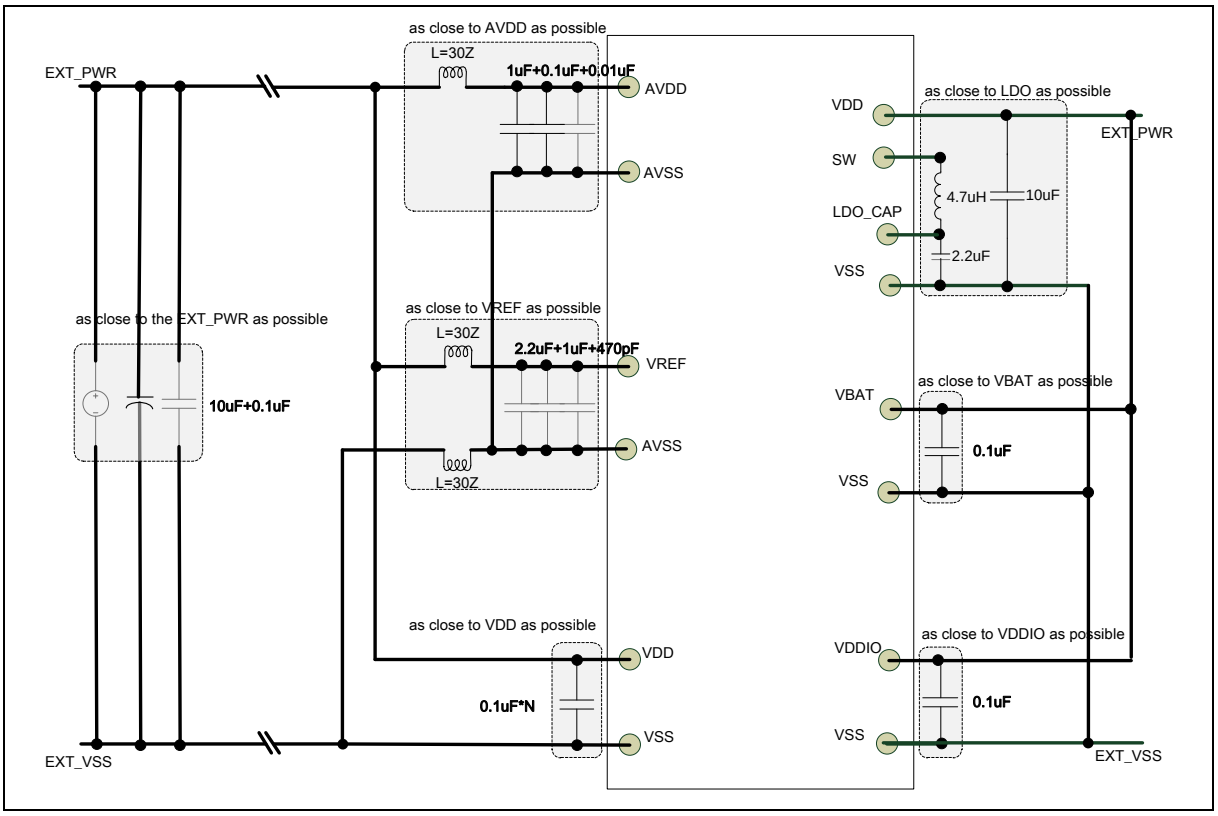
6.44 Peripherals Interconnection

6.44.1 Overview

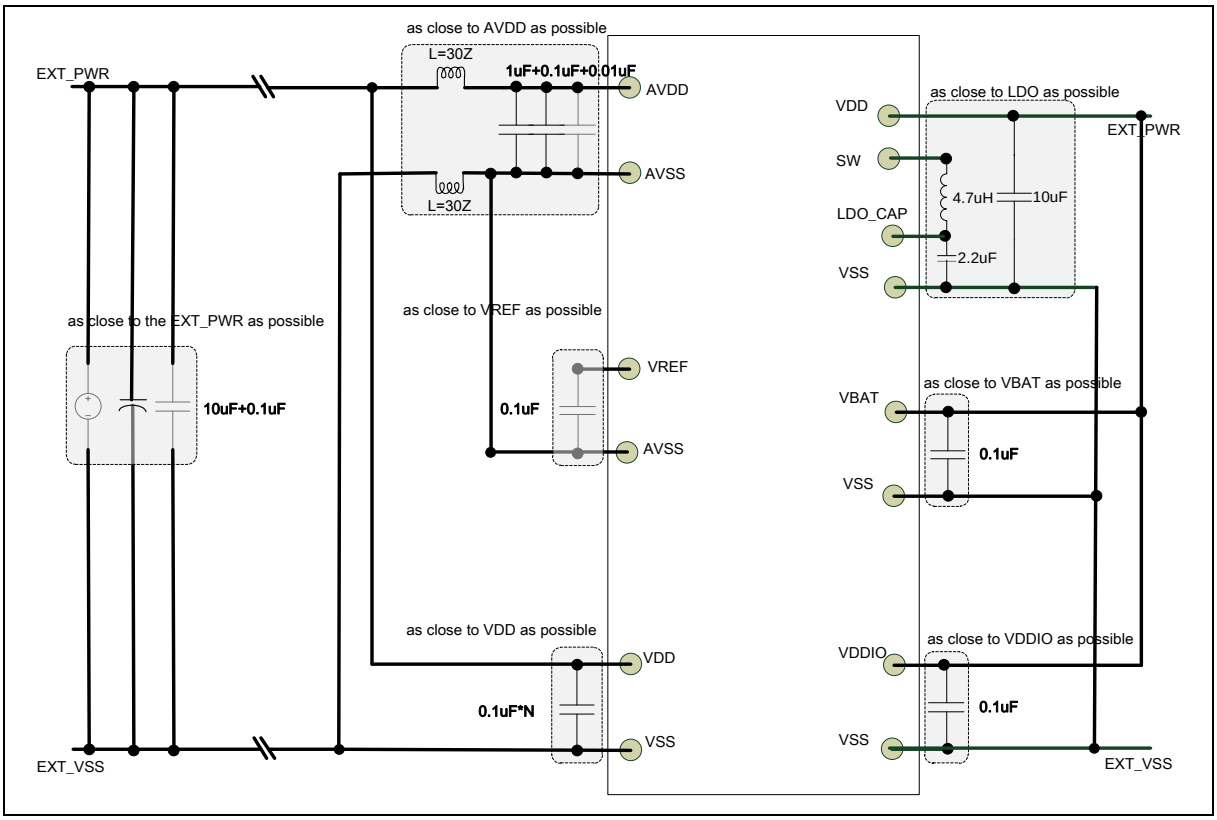
Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast response.

7 APPLICATION CIRCUIT

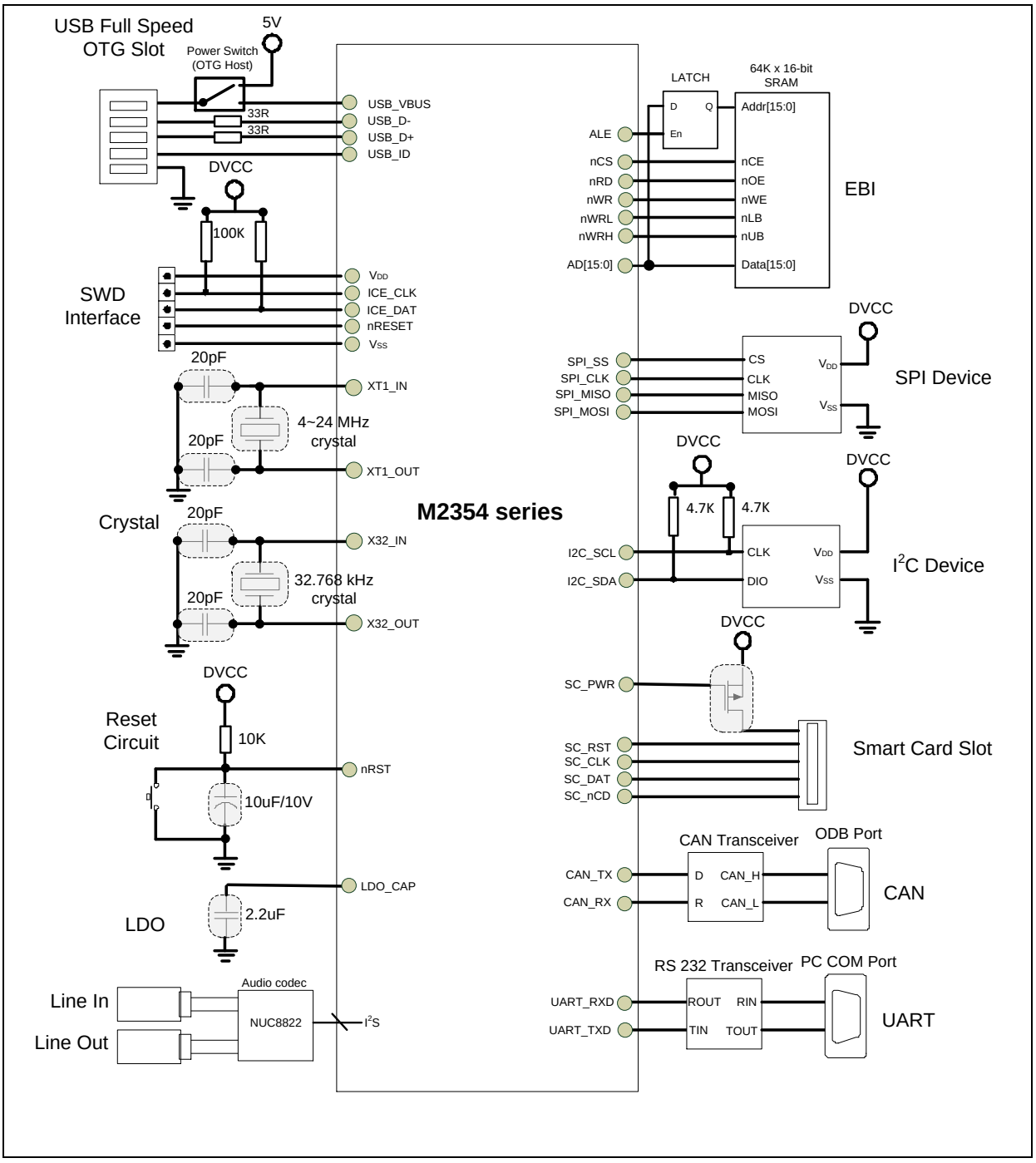
7.1 Power Supply Scheme with External V_{REF}



7.2 Power supply scheme with Internal Vref



7.3 Peripheral Application scheme



*__Note:__ USB_ID, HSUSB _ID could be floating using USB or USB HS without OTG.

8 ELECTRICAL CHARACTERISTIC

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
V_{DDIO}-V_{SS}[*1]	V_{DDIO} Power Supply	-0.3	4.0	V
V_{BAT}-V_{SS}[*1]	V_{BAT} Power Supply	-0.3	4.0	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\lvert V_{SS} - AV_{SS} \rvert$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance GPIO	V_{SS}-0.3	5.5	V
	Input Voltage on RTC domain (PF.6 ~ PF.11)	V_{SS}-0.3	4.0	V
	Input Voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Notes:

1. All main power (V_{DD}, V_{DDIO}, V_{BAT}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Non 5V-tolerance PIN: PA.10, 11, 13 ~ 15; PB.0 ~ 15; PF.2, 3

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	-	100	
I_{BAT}	Maximum Current into V_{BAT}	-	100	
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin

- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  1. Relays, switch contactors
  2. Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-2000	-	2000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-500	-	500	
LU[*3]	Pin current for latch-up[*3]	-400	-	400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing

Pacakge	MSL
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

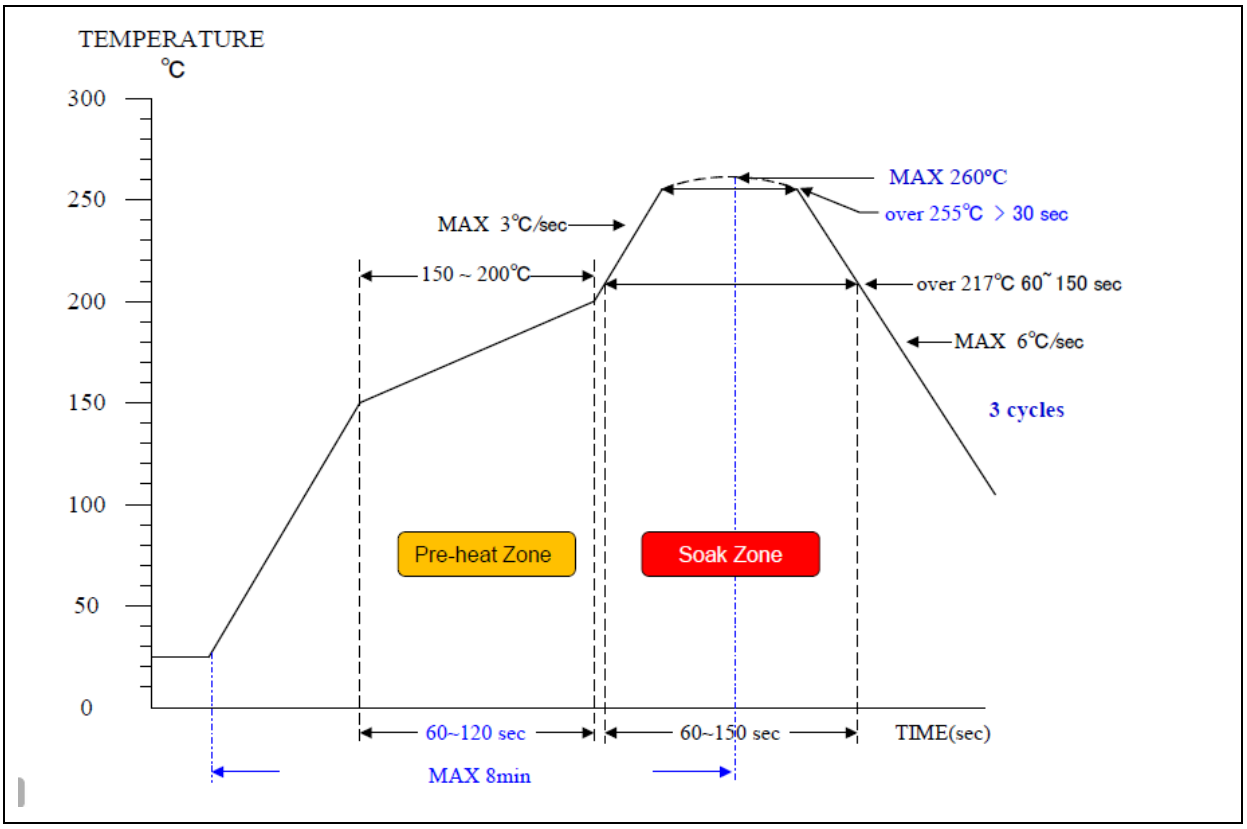


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD} -V_{SS} = 1.7 ~ 3.6V, TA = 25°C, HCLK = 96 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	96	MHz	
V_{DD}	Operation voltage	1.7	-	3.6	V	
V_{DDIO}[*4]	V_{DDIO} Operation voltage	1.7	-	3.6		
V_{BAT}	V_{BAT} Operation voltage	1.7	-	3.6		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.6	-	3.6		
V_{LDO}	LDO output voltage (PL0)	1.134	1.26	1.386		
V_{LDO}	LDO output voltage (PL1)	1.08	1.2	1.32		
V_{LDO}	LDO output voltage (PL2)	0.99	1.1	1.21		
V_{LDO}	LDO output voltage (PL3)	0.81	0.9	0.99		
V_{BG}	Band-gap voltage	1.182	1.200	1.218	mV	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	50	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	4.7			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	100mA	mA	

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in condition and table below to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- F_{HCLK}/ LDO : 96MHz/ 1.26 V (PL0), 84MHz /1.2 V (PL1),
  48MHz-6MHz/ 1.1V (PL2), 4MHz-32KHz/0.9 (PL3)
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

8.3.1.1 LDO Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1] [*2]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance, all peripherals disable	96 MHz	8.58	8.74	11.41	13.67	mA
		84 MHz	7.47	7.57	9.91	11.93	
		48 MHz(PLL)	4.18	4.29	6.12	7.79	
		48MHz(HIRC48)	3.81	3.94	5.66	7.29	
		12 MHz	1.80	1.98	3.76	5.42	
		6 MHz	0.80	0.92	2.64	4.27	
		4 MHz	0.50	0.56	1.63	2.73	
		2 MHz	0.39	0.45	1.52	2.61	
		32.768 KHz	0.16	0.22	1.29	2.38	
		32 KHz	0.16	0.22	1.29	2.38	
	Normal run mode, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance all peripherals enable	96 MHz	27.81	27.97	30.97	33.38	
		84 MHz	23.53	23.64	26.22	28.36	
		48 MHz(PLL)	12.73	12.91	14.89	16.62	
		48MHz(HIRC48)	12.62	12.82	14.54	16.16	
		12 MHz	4.17	4.40	6.22	7.88	
		6 MHz	2.17	2.33	4.11	5.74	
		4 MHz	1.26	1.34	2.45	3.56	
		2 MHz	0.88	0.96	2.06	3.17	
		32.768 KHz	0.34	0.43	1.51	2.62	
		32 KHz	0.34	0.43	1.52	2.62	

Notes:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in LDO Normal Run Mode

8.3.1.2 DC-DC Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1] [*2]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance, all peripherals disable	96 MHz	3.81	3.72	4.75	5.65	mA
		84 MHz	3.19	3.11	3.98	4.76	
		48 MHz(PLL)	1.69	1.70	2.34	2.97	
		48MHz(HIRC48)	1.58	1.60	2.22	2.83	
		12 MHz	1.12	1.22	1.91	2.55	
		6 MHz	0.38	0.42	1.06	1.67	
		4 MHz	0.24	0.26	0.61	0.97	
		2 MHz	0.20	0.22	0.57	0.93	
		32.768 KHz	0.10	0.12	0.47	0.83	
		32 KHz	0.10	0.12	0.47	0.83	
	Normal run mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance all peripherals enable	96 MHz	12.25	11.71	12.82	13.79	
		84 MHz	9.93	9.52	10.43	11.26	
		48 MHz(PLL)	5.01	4.93	5.58	6.22	
		48MHz(HIRC48)	5.00	4.93	5.49	6.09	
		12 MHz	2.05	2.13	2.82	3.45	
		6 MHz	0.91	0.96	1.60	2.21	
		4 MHz	0.49	0.51	0.87	1.22	
		2 MHz	0.36	0.39	0.74	1.11	
		32.768 KHz	0.16	0.19	0.54	0.90	
		32 KHz	0.16	0.19	0.54	0.90	

Notes:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in DC-DC Normal Run Mode

8.3.1.3 LDO Idle Mode

Symbol	Conditions	F_{HCLK}	Typ [*1] [*2]	Max [*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance all peripherals disable	96 MHz	3.03	3.21	5.73	7.92	mA
		84 MHz	2.84	2.97	5.20	7.17	
		48MHz(PLL)	1.75	1.86	3.64	5.28	
		48MHz(HIRC48)	1.39	1.51	3.23	4.85	
		12 MHz	1.20	1.37	3.15	4.80	
		6 MHz	0.50	0.61	2.32	3.94	
		4 MHz	0.33	0.39	1.46	2.55	
		2 MHz	0.31	0.37	1.44	2.52	
		32.768 KHz	0.16	0.22	1.28	2.37	
		32 KHz	0.16	0.22	1.28	2.37	
	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance all peripherals enable	96 MHz	21.39	21.57	24.43	26.77	
		84 MHz	18.17	18.27	20.78	22.87	
		48MHz(PLL)	9.91	10.08	12.00	13.70	
		48MHz(HIRC48)	9.81	10.00	11.72	13.33	
		12 MHz	3.47	3.69	5.50	7.16	
		6 MHz	1.81	1.96	3.73	5.35	
		4 MHz	1.06	1.14	2.24	3.34	
		2 MHz	0.77	0.86	1.95	3.05	
		32.768 KHz	0.34	0.42	1.51	2.60	
		32 KHz	0.34	0.43	1.51	2.60	

Notes:

1. When analog peripheral blocks such as USB, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-3 Current consumption in Idle Mode

8.3.1.4 DC-DC Idle Mode

Symbol	Conditions	F_{HCLK}	Typ [*1] [*2]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance all peripherals disable	96 MHz	1.38	1.41	2.42	3.32	mA
		84 MHz	1.25	1.27	2.12	2.90	
		48MHz(PLL)	0.75	0.78	1.43	2.04	
		48MHz(HIRC48)	0.64	0.68	1.31	1.93	
		12 MHz	0.89	0.99	1.68	2.32	
		6 MHz	0.26	0.31	0.95	1.55	
		4 MHz	0.18	0.20	0.55	0.91	
		2 MHz	0.17	0.20	0.54	0.90	
		32.768 KHz	0.10	0.12	0.47	0.83	
		32 KHz	0.10	0.12	0.47	0.83	
	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance all peripherals enable	96 MHz	9.41	9.05	10.12	11.07	
		84 MHz	7.66	7.36	8.28	9.09	
		48MHz(PLL)	3.91	3.87	4.52	5.14	
		48MHz(HIRC48)	3.91	3.88	4.45	5.04	
		12 MHz	1.77	1.87	2.56	3.19	
		6 MHz	0.77	0.82	1.46	2.07	
		4 MHz	0.42	0.45	0.80	1.16	
		2 MHz	0.33	0.35	0.71	1.07	
		32.768 KHz	0.16	0.19	0.54	0.90	
		32 KHz	0.15	0.19	0.54	0.90	

Notes:

1. When analog peripheral blocks such as USB, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-4 Current Consumption in DC-DC Mode

8.3.1.5 LDO Power-down Mode

Symbol	Conditions	LXT	LIRC	PLL	Power Level	TYP(TA = 25 °C)		MAX(TA = 105 °C)	uint
						1.7V	3.3V	3.6V	
I_{DD_FWPD} [*1]	Fast wake-up Power-down mode, all peripherals disabled	-	-	-	1.26	258.91	274.93	6018.02	uA
					1.2	237.98	245.17	5331.05	
					1.1	200.91	207.21	4501.77	
					0.9	152.19	157.42	3102.77	
	Fast wake-up Power-down mode, RTC/WDT/Timer/UART/LCD enable	V	-	-	1.26	264.62	281.11	5977.2	
					1.2	242.46	250.07	5246.41	
					1.1	203.59	210.15	4326.78	
					0.9	154.04	159.54	3058	
	Fast wake-up Power-down mode, RTC/WDT/Timer/LCD enable	-	V	-	1.26	264.88	281.41	6110.40	
					1.2	242.50	250.11	5456.65	
					1.1	203.48	210.08	4501.67	
					0.9	153.88	159.16	3102.17	
	Fast wake-up Power-down mode, WDT/Timer use LIRC, RTC/UART/LCD use LXT	V	V	-	1.26	266.16	282.84	6020.62	
					1.2	243.87	251.61	5289.56	
					1.1	204.58	211.28	4355.66	
					0.9	154.77	160.33	3071.43	
I_{DD_PD} [*2]	Power-down mode, all peripherals disabled	-	-	-	1.26	62.38	68.59	2324.01	
					1.2	54.12	56.84	2124.82	
					1.1	39.49	41.98	1835.41	
					0.9	21.21	23.52	1371.84	
	Power-down mode, RTC/WDT/Timer/UART/LCD enable	V	-	-	1.26	64.17	70.57	2321.26	
					1.2	55.81	58.65	2130.86	
					1.1	41.22	43.86	1835.89	
					0.9	22.71	25.24	1377.10	
	Power-down mode, RTC/WDT/Timer/LCD use LIRC	-	V	-	1.26	63.79	70.21	2326.18	
					1.2	55.49	58.40	2125.00	
					1.1	40.72	43.45	1831.83	
					0.9	22.36	24.86	1365.45	
	Power-down mode,	V	V	-	1.26	65.07	71.65	2328.08	

	WDT/Timer use LIRC; RTC/UART/LCD use LXT				1.2	56.74	59.79	2135.45
					1.1	41.92	44.71	1842.56
					0.9	23.54	26.19	1369.26
I_{DD_LLPD} [*2]	Low leakage Power-down mode, all peripherals disabled	-	-	-	0.9	24.72	27.08	1472.53
	Low leakage Power-down mode, RTC/WDT/Timer/UART enabled	V	-	-	0.9	26.31	28.84	1475.95
	Low leakage Power-down mode, RTC/WDT/Timer enabled	-	V	-	0.9	25.87	28.30	1476.47
	Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT	V	V	-	0.9	26.86	29.47	1477.57
I_{DD_ULLPD} [*2]	Ultra Low leakage Power-down mode, all peripherals disabled	-	-	-	0.8	17.77	20.09	1276.98
	Ultra Low leakage Power-down mode, RTC/WDT/Timer/UART enabled	V	-	-	0.8	19.34	21.72	1279.30
	Ultra Low leakage Power-down mode, RTC/WDT/Timer enabled	-	V	-	0.8	18.80	21.30	1273.86
	Ultra Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT	V	V	-	0.8	19.81	22.35	1281.99
I_{DD_SPD} [*2]	Standby Power-down mode(SPD), all peripherals disabled	-	-	-	1.26	85.66	91.24	2774.68
					1.2	72.97	74.33	2491.50
					1.1	52.35	53.43	2079.19
					0.9	26.79	27.57	1428.54
	Standby Power-down mode(SPD), RTC enabled	V	-	-	1.26	86.57	92.33	2776.79
					1.2	73.92	75.48	2490.83
					1.1	53.13	54.40	2079.97

					0.9	27.65	28.53	1432.11	
	Standby Power-down mode (SPD), RTC enabled	-	V	-	1.26	86.01	91.75	2794.27	
					1.2	73.56	75.00	2494.63	
					1.1	52.75	53.97	2075.51	
					0.9	27.11	28.02	1425.21	
I_{DD_SPD2} [*3]	Standby Power-down mode (SPD), all peripherals disabled	-	-	-	1.26	3.86	4.55	123.93	
					1.2	3.44	3.97	113.76	
					1.1	2.71	3.23	99.16	
					0.9	1.71	2.23	78.78	
	Standby Power-down mode (SPD), RTC enabled	V	-	-	1.26	4.73	5.58	126.01	
					1.2	4.31	5.01	115.31	
					1.1	3.58	4.27	101.21	
					0.9	2.58	3.26	80.32	
	Standby Power-down mode (SPD), RTC enabled	-	V	-	1.26	4.26	5.08	124.88	
					1.2	3.84	4.51	114.30	
					1.1	3.11	3.77	100.33	
					0.9	2.11	2.76	79.82	
I_{DD_DPD} [*4]	Deep Power-down mode(DPD), all peripherals disabled	-	-	-	Floating	0.07	0.48	19.14	
	Deep Power-down mode(DPD), RTC enabled	V	-	-	Floating	0.93	1.50	20.51	
	Deep Power-down mode (DPD), RTC enabled	-	V	-	Floating	0.06	0.47	19.06	

Notes:

1. All sram banks keep as normal mode.
2. All sram banks put into retention mode by hardware.
3. Only bank0 sram0(4k) keep as retention mode, others set as shut down mode.
4. All sram are in power shut down mode.

Table 8.3-5 Chip Current Consumption in LDO Power-down Mode

8.3.1.6 DC-DC Power-down Mode

Symbol	Conditions	LXT	LIRC	PLL	Power Level	TYP(TA = 25 °C)		MAX(TA = 105 °C)	uint
						1.7V	3.3V	3.6V	
I_{DD_FWPD} [*1]	Fast wake-up Power-down mode, all peripherals disabled	-	-	-	1.26	231.27	155.29	2045.03	uA
					1.2	201.00	137.95	1755.97	
					1.1	153.86	117.09	1386.10	
					0.9	106.86	93.33	810.34	
	Fast wake-up Power-down mode, RTC/WDT/Timer/UART/LCD enable	V	-	-	1.26	231.69	155.86	2100.01	
					1.2	203.22	139.60	1783.92	
					1.1	156.89	119.17	1401.13	
					0.9	109.37	95.21	817.92	
	Fast wake-up Power-down mode, RTC/WDT/Timer/LCD enable	-	V	-	1.26	236.18	157.98	2097.15	
					1.2	206.94	141.13	1788.92	
					1.1	159.08	120.16	1410.10	
					0.9	110.21	95.52	819.93	
	Fast wake-up Power-down mode, WDT/Timer use LIRC, RTC/UART/LCD use LXT	V	V	-	1.26	241.40	161.38	2113.30	
					1.2	211.04	143.74	1792.01	
					1.1	162.05	122.20	1411.26	
					0.9	112.04	97.10	822.89	
I_{DD_PD} [*2]	Power-down mode, all peripherals disabled	-	-	-	1.26	73.40	40.60	742.08	
					1.2	61.49	33.20	640.11	
					1.1	40.24	23.86	516.23	
					0.9	18.72	12.96	316.42	
	Power-down mode, RTC/WDT/Timer/UART/LCD enable	V	-	-	1.26	75.78	42.39	744.41	
					1.2	63.34	34.62	643.06	
					1.1	41.88	25.24	518.44	
					0.9	20.06	14.21	318.96	
	Power-down mode, RTC/WDT/Timer/LCD use LIRC	-	V	-	1.26	76.05	42.38	743.49	
					1.2	63.61	34.66	643.01	
					1.1	41.87	25.04	517.96	
					0.9	19.80	13.85	318.33	
	Power-down mode,	V	V	-	1.26	77.30	43.56	746.19	

	WDT/Timer use LIRC, RTC/UART/LCD use LXT				1.2	65.02	35.88	645.97
					1.1	43.28	26.26	520.28
					0.9	21.09	15.14	319.84
I_{DD_LLPD} [*2]	Low leakage Power-down mode, all peripherals disabled	-	-	-	0.9	19.30	13.25	317.03
	Low leakage Power-down mode, RTC/WDT/Timer/UART enable	V	-	-	0.9	20.64	14.54	319.06
	Low leakage Power-down mode, RTC/WDT/Timer enable	-	V	-	0.9	20.09	14.03	318.37
	Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT	V	V	-	0.9	20.96	14.93	320.79
I_{DD_ULLPD} [*2]	Ultra Low leakage Power-down mode, all peripherals disabled	-	-	-	0.8	12.76	9.91	244.62
	Ultra Low leakage Power-down mode, RTC/WDT/Timer/UART enable	V	-	-	0.8	13.96	11.18	246.49
	Ultra Low leakage Power-down mode, RTC/WDT/Timer enable	-	V	-	0.8	13.52	10.74	245.57
	Ultra Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT	V	V	-	0.8	14.50	11.79	247.25
I_{DD_SPD} [*2]	Standby Power-down mode(SPD), all peripherals disabled	-	-	-	1.26	108.38	55.40	1188.96
					1.2	88.16	43.81	1008.70
					1.1	56.42	29.75	776.52
					0.9	24.20	13.44	420.41
	Standby Power-down mode(SPD), RTC enable	V	-	-	1.26	109.22	56.41	1199.34
					1.2	89.02	44.88	1009.90
					1.1	57.11	30.71	778.44

					0.9	24.97	14.43	422.16	
	Standby Power-down mode(SPD), RTC enable	-	V	-	1.26	108.26	55.67	1195.08	
					1.2	88.35	44.19	1009.44	
					1.1	56.57	30.15	778.36	
					0.9	24.46	13.92	421.71	
I_{DD_SPD2} [*3]	Standby Power-down mode(SPD), all peripherals disabled	-	-	-	1.26	4.35	3.00	58.97	
					1.2	3.73	2.62	52.88	
					1.1	2.62	2.14	45.03	
					0.9	1.43	1.53	33.05	
	Standby Power-down mode(SPD), RTC enable	V	-	-	1.26	5.25	4.03	60.32	
					1.2	4.59	3.65	54.04	
					1.1	3.48	3.17	46.59	
					0.9	2.31	2.58	34.78	
	Standby Power-down mode(SPD), RTC enable	-	V	-	1.26	4.72	3.52	59.67	
					1.2	4.09	3.15	53.64	
					1.1	2.99	2.66	46.08	
					0.9	1.83	2.06	33.94	
I_{DD_DPD} [*4]	Deep Power-down mode(DPD), all peripherals disabled	-	-	-	Floating	0.06	0.54	18.14	
	Deep Power-down mode(DPD), RTC enable	V	-	-	Floating	0.94	1.57	19.06	
	Deep Power-down mode(DPD), RTC enable	-	V	-	Floating	0.06	0.53	17.86	

Notes:

1. All sram banks keep as normal mode.
2. All sram banks put into retention mode by hardware.
3. Only bank0 sram0(4k) keep as retention mode, others set as shut down mode.
4. All sram are in power shut down mode.

Table 8.3-6 Chip Current Consumption in DC-DC Power-down Mode

8.3.1.7 Current Consumption for RTC Domain

Symbol	Conditions	LXT	T_A	LDO	DCDC	Unit
I_{BAT}	RTC enabled, operating current, V_{BAT} = 3.6V	V	-40 °C	1.08	1.08	uA
			25 °C	1.97	2.12	
			55 °C	3.93	3.92	
			85 °C	8.19	8.09	
			105 °C	12.94	12.99	
	RTC enabled, operating current, V_{BAT} = 3.3V	V	-40 °C	1.00	1.00	
			25 °C	1.42	1.49	
			55 °C	2.38	2.38	
			85 °C	4.81	4.79	
			105 °C	7.93	7.96	
	RTC enabled, operating current, V_{BAT} = 1.7V	V	-40 °C	0.80	0.80	
			25 °C	0.98	0.99	
			55 °C	1.10	1.10	
			85 °C	1.35	1.36	
			105 °C	1.66	1.70	
	RTC disabled, operating current, V_{BAT} = 3.6V	V	-40 °C	0.11	0.11	
			25 °C	0.89	1.01	
			55 °C	2.76	2.75	
			85 °C	6.92	6.91	
			105 °C	11.65	11.51	
	RTC disabled, operating current, V_{BAT} = 3.3V	V	-40 °C	0.09	0.09	
			25 °C	0.39	0.44	
			55 °C	1.27	1.27	
			85 °C	3.63	3.62	
			105 °C	6.67	6.53	
	RTC disabled, operating current, V_{BAT} = 1.7V	V	-40 °C	0.08	0.08	
			25 °C	0.11	0.11	
			55 °C	0.15	0.15	
			85 °C	0.31	0.31	
			105 °C	0.59	0.51	

Note: Guaranteed by characterization results, not tested in production.

Table 8.3-7 Chip Current Consumption for RTC

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function
- LDO = 1.26.
- HCLK is the system clock, f_{HCLK} = 96 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA0	422	uA
PDMA1	423	
ISP	0	
EBI	266	
EXST	158	
SDH0	1452	
CRC	200	
CRPT	259	
KS	463	
TRACE	6	
FMC	304	
USBH	1248	
SRAM0	201	
SRAM1	462	
SRAM2	361	
GPA	85	
GPB	254	
GPC	251	
GPD	263	
GPE	256	
GPF	237	
GPG	236	
GPH	232	
WDT	633	

RTC	189	
TMR0	770	
TMR1	788	
TMR2	455	
TMR3	487	
CLKO	192	
ACMP01	253	
I2C0	573	
I2C1	258	
I2C2	559	
QSPI0	1430	
SPI0	812	
SPI1	1346	
SPI2	827	
UART0	1401	
UART1	937	
UART2	1285	
UART3	775	
UART4	1221	
UART5	779	
TAMPER	514	
CAN0	713	
OTG	981	
USBD	1298	
EADC	562	
I2S0	1107	
EWDT	649	
SC0	986	
SC1	605	
SC2	1005	
TMR4	831	
TMR5	829	
SPI3	1372	

USCI0	605	
USCI1	272	
DAC	212	
EPWM0	767	
EPWM1	459	
BPWM0	576	
BPWM1	230	
QEI0	548	
QEI1	225	
LCD	266	
TRNG	1036	
ECAP0	547	
ECAP1	217	
LCDFC	4	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 8.3-8 Peripheral Current Consumption

8.3.3 Wakeup Timefrom Low-Power Modes

- The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 12 MHz HIRC oscillator. The clock source used to wake up the device depends from the current operating mode:
  - Fast-wakeup, power down, low leakage Power-down mode: the clock source is the RC oscillator
  - Standby and Deep Power-down mode: the clock source is the clock that was set before entering Sleep mode.
- The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
- The clock source is the RC oscillator from HIRC

Symbol	Parameter	Typ	Unit
t_{WU_IDLE}[*1]	Wakeup from IDLE mode	0.835	µs
t_{WU_FWPD}[*1]	Wakeup from Fast-wakeup Power-down mode	9.795	
t_{WU_NPD}[*1]	Wakeup from normal Power-down mode	21.295	
t_{WU_LLPD}[*1]	Wakeup from low leakage Power-down mode	68.995	

t_{WU_ULLPD}[*1]	Wakeup from ultra low leakage power down	67.875	
t_{WU_SPD}[*1]	Wakeup from Standby Power-down mode (SPD)	226.4	
t_{WU_DPD}[*1]	Deep Power-down mode (DPD)	10445	
t_{ET_IDLE}[*2]	Enter to IDLE mode	0.5	µs
t_{ET_DPD}[*2]	Enter to deep Power-down mode	95.695	
t_{ET_SPD}[*2]	Enter to standby Power-down mode	55.34	
t_{ET_ULLPD}[*2]	Enter to ultra low Power-down mode	56.458	
t_{ET_LLPD}[*2]	Enter to low Power-down mode	56.178	
t_{ET_NPD}[*2]	Enter to normal Power-down mode	5.912	
t_{ET_FWPD}[*2]	Enter to fast wake-up Power-down mode	5.495	

Note:

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by Design
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-9 Low-power Mode Wakeup Timings

8.3.4 I/O DC Characteristics

8.3.4.1 PIN input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL1}	Input Low Voltage (TTL input)	-	-	0.8	V	$V_{DD} = V_{DDIO} = 3.6$ V
		-	-	0.7	V	$V_{DD} = V_{DDIO} = 1.7$ V
V_{IH1}	Input High Voltage (TTL input)	2.0	-	-	V	$V_{DD} = V_{DDIO} = 3.6$V
		1.0	-	-	V	$V_{DD} = V_{DDIO} = 1.7$V
V_{IL2}	Input Low Voltage (Schmitt input)	-	-	$0.3*V_{DD}$	V	$V_{DD} = V_{DDIO} = 3.6$V
		-	-	$0.3*V_{DD}$		$V_{DD} = V_{DDIO} = 1.7$V
V_{IH2}	Input High Voltage (Schmitt input)	$0.7*V_{DD}$	-	-	V	$V_{DD} = V_{DDIO} = 3.6$V
		$0.7*V_{DD}$	-	-		$V_{DD} = V_{DDIO} = 1.7$V
V_{HY}[*1]	Hysteresis voltage of (Schmitt input)	-	0.75	-	V	V_{DD} =3.6V
I_{LK}[*2]	Input Leakage Current	-1	-	1	µA	$V_{DD} = V_{DDIO} = 3.6$V, $0 < V_{IN} < V_{DD}$, Open-drain or input only mode
I_{IL}	Logic 0 Input Current (Quasi-bidirectional mode)		69		uA	$V_{DD} = V_{DDIO} = 3.6$V, $V_{IN} = 0$V
R_{PU}[*1]	Input Pull Up Resistor	-	52	-	KΩ	$V_{DD} = V_{DDIO} = 3.3$V
		-	53	-	KΩ	$V_{DD} = V_{DDIO} = 1.8$V
R_{PD}[*1]	Input Pull down Resistor	-	52	-	KΩ	$V_{DD} = V_{DDIO} = 3.3$V
		-	53	-	KΩ	$V_{DD} = V_{DDIO} = 1.8$V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-10 I/O Input Characteristics

8.3.4.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR1}[*1] [*2]	Source Current (Quasi-bidirectional Mode, Set GPIO to output HIGH, Apply GPIO pin V_{IN}=(V_{DD}-0.4)V for V_{DD} and measure the source current)	7.66	-	7.86	uA	V_{DD} = V_{DDIO} = 3.3V V_{IN}=(V_{DD}-0.4) V
I_{SR2}[*1] [*2]		7.51	-	7.69	uA	V_{DD} = V_{DDIO} = 1.8V V_{IN}=(V_{DD}-0.4) V
I_{SR3}[*1] [*2]	Source Current (Push-pull Mode, Set GPIO to output HIGH, Apply GPIO pin VIN=(V_{DD}-0.4)V for V_{DD} and measure the source current)	18.1	-	18.98	mA	V_{DD} = V_{DDIO} = 3.3V V_{IN}=(V_{DD}-0.4) V
I_{SR4}[*1] [*2]		10.04	-	10.79	mA	V_{DD} = V_{DDIO} = 1.8V V_{IN}=(V_{DD}-0.4) V
I_{SK1}[*1] [*2]	Sink Current (Quasi-bidirectional, Push-pull Mode, Set GPIO to output LOW, Apply GPIO pin VIN=(V_{SS}+0.4)V for V_{SS} and measure the source current)	17.10	-	17.75	mA	V_{DD} = V_{DDIO} = 3.3V V_{IN}= 0.4 V
I_{SK2}[*1] [*2]		10.44	-	10.83	mA	V_{DD} = V_{DDIO} = 1.8V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	4.2	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The ISR and ISK must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣIDD and ΣISS.

Table 8.3-11 I/O Output Characteristics

8.3.4.3 nRESET Output Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	unit	Test Conditions
V_{ILR}	Negative going threshold (Schmitt input), nRESET	-	-	0.3*V_{DD}	V	V_{DD} = 3.3V
V_{IHR}	Positive going threshold (Schmitt Input), nRESET	0.7*V_{DD}	-	-	V	V_{DD} = 3.3V
R_{RST}[*1]	Internal nRESET pin pull up resistor	53.40	54	54.51	KΩ	
t_{FR1}[*1]	nRESET input filtered time	-	32	-	uS	V_{DD} = 3.3V
	nRESET input filtered time under FWPD mode	-	32	-		
	nRESET input filtered time under PD mode	-	32	-		
	nRESET input filtered time under LLPD mode	-	32	-		
	nRESET input filtered time under ULLPD mode	-	32	-		

	nRESET input filtered time under SPD mode	-	0	-		
	nRESET input filtered time under DPD mode	-	0	-		

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-12 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 12MHz Internal High Speed RC Oscillator (HIRC)

Symbol.	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	3	3.6	V	
f_{HRC}	Oscillator frequnecy	-	12	-	MHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-0.25	-	+0.25	%	T_A = 25 °C, V_{DD} = 3.3 V
		-4	-	+4	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V
I_{HRC}[*1]	Operating current	-	50	70	µA	
T_S[*2]	Stable time	-	-	20	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.2 48MHz Internal High Speed RC Oscillator (HIRC48)

Symbol.	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	3.3	3.6	V	
f_{HRC}	Oscillator frequnecy	-	48	-	MHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-0.25	-	+0.25	%	T_A = 25 °C, V_{DD} = 3.3 V
		-4	-	+4	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V
I_{HRC}[*1]	Operating current		146	230	µA	
T_S[*2]	Stable time	-	-	20	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V

Notes:
1. Guaranteed by characterization result, not tested in production
2. Guaranteed by design.

Table 8.4-2 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.3 32 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	3	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	32	-	kHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-0.4	-	+0.4	%	T_A = 25 °C, V_{DD} = 3.3 V
		-15	-	+15	%	T_A=-40~105°C V_{DD}=1.7V~3.6V
I_{LRC} [*1]	Operating current	-	0.6	0.8	µA	V_{DD} = 3.3V
T_S [*2]	Stable time	-	-	500	µs	T_A=-40~105°C V_{DD}=1.7V~3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design.

Table 8.4-3 32 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.4 32kHz Internal Low Speed RC Oscillator in V_{BAT} domain (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	3	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	32	-	kHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-0.4	-	+0.4	%	T_A = 25 °C, V_{DD} = 3.3 V
		-15	-	+15	%	T_A=-40~105°C V_{DD}=1.7V~3.6V
I_{LRC} [*1]	Operating current	-	0.6	0.8	µA	V_{DD} = 3.3V
T_S [*2]	Stable time	-	-	500	µs	T_A=-40~105°C V_{DD}=1.7V~3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design.

Table 8.4-4 32 kHz Internal Low Speed RC Oscillator(LIRC_ V_{BAT}) Characteristics

8.4.5 4MHz internal medium speed RC oscillator (MIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	3	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	4	-	MHz	T_A = 25 °C, V_{DD} = 3.3 V

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
	Frequency drift over temperarure and volatge	-0.25	-	+0.25	%	T_A = 25 °C, V_{DD} = 3.3 V
		-4	-	+4	%	T_A=-40~105°C V_{DD}=1.7V~3.6V
I_{LRC} [*1]	Operating current	-	70	85	μA	V_{DD} = 3.3V
T_S [*2]	Stable time	-	-	20	μs	T_A=-40~105°C V_{DD}=1.7V~3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design.

Table 8.4-5 4 MHz Internal Medium Speed RC Oscillator (MIRC) Characteristics

8.4.6 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7		3.6	V	
R_f	Internal feedback resister	-	1000	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
T_{HXT}	Temperature Range	-40	-	105	°C	
I_{HXT}	Current consumption	-	250	300	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	400	450		12 MHz, Gain = L1, C_L = 12.5 pF
		-	500	560		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	640	720		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time	-	-	1802	μs	4 MHz, Gain = L0, C_L = 12.5 pF
		-	-	560		12 MHz, Gain = L1, C_L = 12.5 pF
		-	-	408		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	-	348		24 MHz, Gain = L3, C_L = 12.5 pF
Du_{HXT}	Duty cycle	45	50	55	%	

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	120	400	Ω	4 MHz, Gain = L0, C_L = 12.5 pF
		-	25	100		12 MHz, Gain = L1, C_L = 12.5 pF
		-	25	75		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	25	50		24 MHz, Gain = L3, C_L = 12.5 pF

Notes:

1. Guaranteed by characterization, not tested in production.
2. $C_L = \frac{1}{\frac{1}{C1}+\frac{1}{C2}} + Cparasitic$.
3. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD}+R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

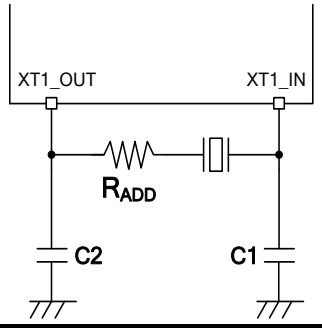


Table 8.4-6 External 4~24 MHz High Speed Crystal (HXT) Oscillator

8.4.6.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	20pF	20pF	without

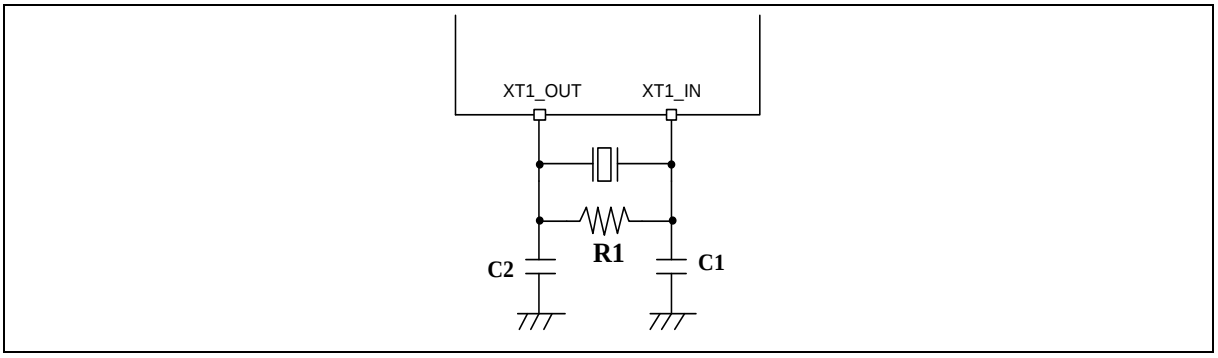
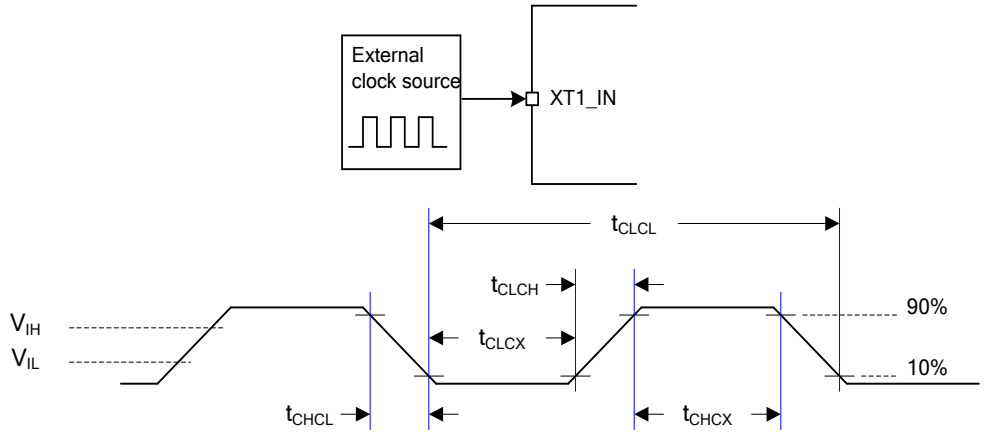


Figure 8.4-1 Typical Crystal Application Circuit

8.4.7 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal needs to follow Table 8.4-7. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	0.032768	-	24	MHz	
t_{CHCX}	Clock high time	18	-	-	ns	
t_{CLCX}	Clock low time	18	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.
2. Duty cycle is 50%.

Table 8.4-7 External 4~24 MHz High Speed Clock Input Signal

8.4.8 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	1.7	-	3.6	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	6.35	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	130	270	750	nA	ESR=35 kΩ, C_L = 6 pF, Gain = L1
		195	390	960		ESR=35 kΩ, C_L = 12.5 pF, Gain = L3
		230	450	1060		ESR=35 kΩ, C_L = 12.5 pF, Gain = L4
		370	680	1500		ESR=70 kΩ, C_L = 12.5 pF, Gain = L6
		500	920	1950		ESR=70 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	-	2000	ms	
Du_{LXT}	Duty cycle	30	50	70	%	
Vpp	Peak-to-peak amplitude	-	0.557	-	V	V_{DD} =3.3V，L7
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Notes:

1. Guaranteed by characterization, not tested in production.
2. Not supported gain = L0/ L2/ L5
3. $C_L = \frac{1}{\frac{1}{C1}+\frac{1}{C2}} + Cparasitic$.

Table 8.4-8 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

8.4.8.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	20pF	20pF	without

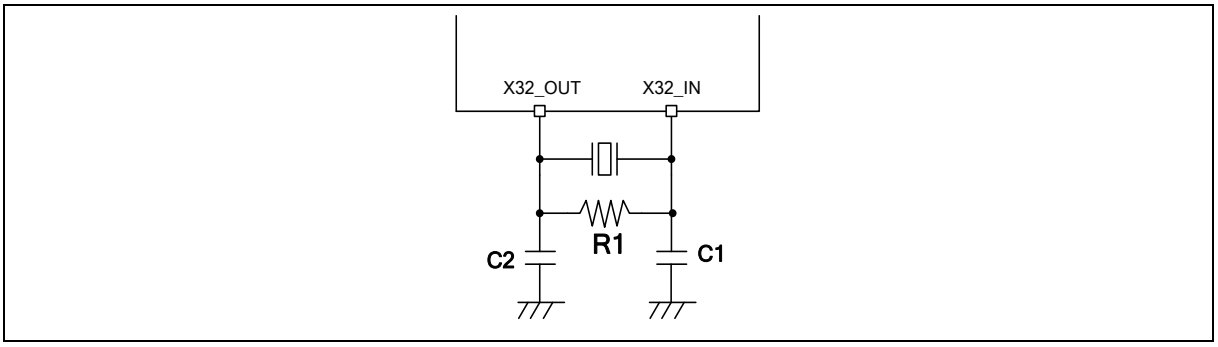
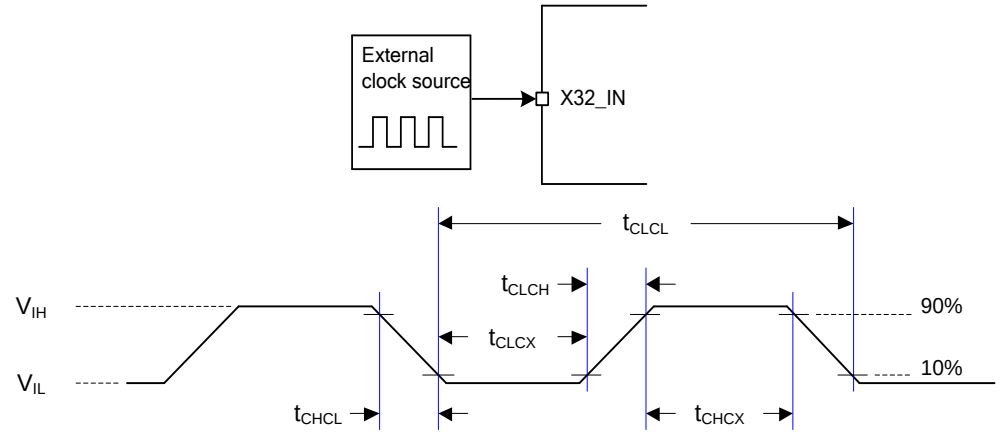


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.9 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal needs to follow Table 8.4-9. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-9 External 32.768 kHz Low Speed Clock Input Signal

8.4.10 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	24	-	200	MHz	
f_{PLL_REF}	PLL reference clock	2	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	96	-	200	MHz	
T_L	PLL locking time	-	-	100	µs	
Jitter	Cycle-to-cycle Jitter	-	250	-	ps	Peak to peak @ 200MHz
I_{DD}	Power consumption	-	0.9	-	mA	V_{DD} =3.3V @ f_{PLL_VCO} = 200 MHz

Notes:

1. Guaranteed by design, not tested in production

Table 8.4-10 PLL Characteristics

8.4.11 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	4.09	ns	V_{DD} = 3.6 V ,C_L = 51 pF
		-	3.23		V_{DD} = 3.6 V ,C_L = 30 pF
		-	10.05		V_{DD} = 1.7 V, C_L = 51 pF
		-	7.82		V_{DD} = 1.7 V, C_L = 30 pF
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	3.47		V_{DD} = 3.6 V ,C_L = 51 pF
		-	2.45		V_{DD} = 3.6 V ,C_L = 30 pF
		-	7.37		V_{DD} = 1.7 V, C_L = 51 pF
		-	5.96		V_{DD} = 1.7 V, C_L = 30 pF
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	4.14	ns	V_{DD} = 3.6 V ,C_L = 51 pF
		-	3.32		V_{DD} = 3.6 V ,C_L = 30 pF
		-	9.3		V_{DD} = 1.7 V, C_L = 51 pF
		-	7.5		V_{DD} = 1.7 V, C_L = 30 pF
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	3.08	ns	V_{DD} = 3.6 V ,C_L = 51 pF
		-	2.17		V_{DD} = 3.6 V ,C_L = 30 pF
		-	6.3		V_{DD} = 1.7 V, C_L = 51 pF

		-	4.73		V_{DD} = 1.7 V, C_L = 30 pF
$f_{max(IO)out}$ [*3]	I/O maximum frequency (Normal Slew Rate)	-	81	MHz	V_{DD} = 3.6 V ,C_L = 51 pF
		-	101.7		V_{DD} = 3.6 V ,C_L = 30 pF
		-	34.4		V_{DD} = 1.7 V, C_L = 51 pF
		-	43.5		V_{DD} = 1.7 V, C_L = 30 pF
	I/O maximum frequency (High Slew Rate)	-	101.7	MHz	V_{DD} = 3.6 V ,C_L = 51 pF
		-	144.3		V_{DD} = 3.6 V ,C_L = 30 pF
		-	48.7		V_{DD} = 1.7 V, C_L = 51 pF
		-	62.3		V_{DD} = 1.7 V, C_L = 30 pF

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.

Table 8.4-11 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	1.7	-	3.6	V	
V_{LDO}	Output Voltage	1.134	1.26	1.386	V	Turbo mode[4]
		1.08	1.2	1.32	V	Normal run mode
		0.99	1.1	1.21	V	Normal run mode
		0.81	0.9	0.99	V	Low Power Normal run mode
		-	0.8	-	V	Ultra low leakage Power-down mode
I_{OUT_MAX}	Maximum Output Current	-	-	50	mA	V_{IN}>1.7V
T_A	Temperature	-40	-	125	℃	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 4.7μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.
4. Trubo mode is availabe when V_{DD} between 1.8V~3.6V

Table 8.5-1 LDO Characteristics

8.5.2 DC-DC

Typical values are at V_{DD} = 3.3V, TA = 25°C, Vsw is connected to 4.7uH inductance and LDO_CAP is connected to 4.7uF capacitance unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IN}	Input Voltage Range	1.7	-	3.6	V	
V_{OUT}	Output Voltage Range	1.134	1.26	1.386	V	Turbo mode[3]
		1.08	1.2	1.32	V	Normal run mode
		0.99	1.1	1.21	V	Normal run mode
		0.81	0.9	0.99	V	Low Power Normal run mode
		-	0.8	-	V	Ultra low leakage Power-down mode
I_{OUT_MAX}	Maximum DC Output Current	-	-	50	mA	V_{IN}>1.7V
I_{Q_DCDC}	Quiescent Current	-	4	6	uA	No load, normal mode, only buck regulator
V_{LINE}	Line Regulation	-5	-	+5	%	I_{OUT}=30mA, V_{IN}=1.7V to 3.6V

V_{LOAD}	Load Regulation	-5	-	+5	%	I_{OUT}=0.2mA to 30mA
P_{EFF}	Power Efficiency	-	80	-	%	I_{OUT}= 2~30mA L_{OUT} = 4.7uH, DCR ≤ 180mΩ

Note:

1. It is recommended a 2.2μF and 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 4.7μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. Trubo mode is availabe when V_{DD} between 1.8V~3.6V

Table 8.5-2 LDO Characteristics

8.5.3 Low-Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	1.45	-	3.6	V	
T_A	Temperature	-40	25	125	℃	-
I_{LVR}	Operating Current	-	0.3	0.6	uA	AV_{DD} = 3.6V (BOD_EN = 0)
V_{LVR*}	Threshold Voltage	1.45	1.50	1.65	V	
I_{BOD}	Operating Current	-	30	40	μA	AV_{DD} = 3.6V
V_{BOD_F}	Brown-out Voltage (Falling edge)	2.90	3.00	3.10	V	BODVL (SYS_BODCTL[18:16]) = 111
		2.70	2.80	2.90	V	BODVL (SYS_BODCTL[18:16]) = 110
		2.50	2.60	2.70	V	BODVL (SYS_BODCTL[18:16]) = 101
		2.30	2.40	2.50	V	BODVL (SYS_BODCTL[18:16]) = 100
		2.10	2.20	2.30	V	BODVL (SYS_BODCTL[18:16]) = 011
		1.90	2.00	2.10	V	BODVL (SYS_BODCTL[18:16]) = 010
		1.70	1.80	1.90	V	BODVL (SYS_BODCTL[18:16]) = 001
		1.50	1.60	1.70	V	BODVL (SYS_BODCTL[18:16]) = 000
V_{BOD_R}	Brown-out Voltage (Rising edge)	2.98	3.08	3.18	V	BODVL (SYS_BODCTL[18:16]) = 111
		2.78	2.88	2.98	V	BODVL (SYS_BODCTL[18:16]) = 110
		2.58	2.68	2.78	V	BODVL (SYS_BODCTL[18:16]) = 101
		2.38	2.48	2.58	V	BODVL (SYS_BODCTL[18:16]) = 100

		2.18	2.28	2.38	V	BODVL (SYS_BODCTL[18:16]) = 011
		1.98	2.08	2.18	V	BODVL (SYS_BODCTL[18:16]) = 010
		1.78	1.88	1.98	V	BODVL (SYS_BODCTL[18:16]) = 001
		1.58	1.68	1.78	V	BODVL (SYS_BODCTL[18:16]) = 000
T_{BOD_RE}	Respond Time	-	-	0.03	ms	Sampled by LIRC *1
T_{LVR_RE}	Respond Time	-	-	20	us	
V_{POR}	Reset Voltage	1.38	1.46	1.54	V	
RRV_{DD}	V_{DD} Raising Rate to Ensure Power-on Reset	10	-	-	us/V	POR Enabled
FRV_{DD}	V_{DD} Falling Rate to Ensure Power-on Reset	10	-	-	us/V	LVR Enabled
		200	-	-		BOD 1.6V Enabled, Normal mode
		90	-	-		BOD 1.8V Enabled, Normal mode
		60	-	-		BOD 2.0V Enabled, Normal mode
		40	-	-		BOD 2.2V Enabled, Normal mode
		35	-	-		BOD 2.4V Enabled, Normal mode
		30	-	-		BOD 2.6V Enabled, Normal mode
		25	-	-		BOD 2.8V Enabled, Normal mode
		20	-	-		BOD 3.0V Enabled, Normal mode
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	10	-	-	us	

Note :

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-3 LVR Characteristics

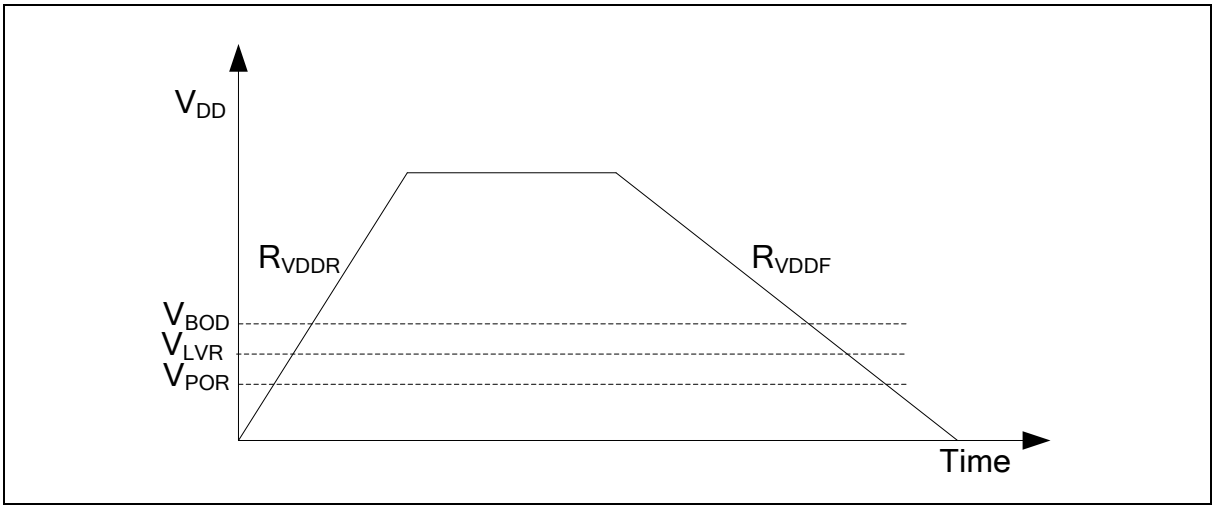


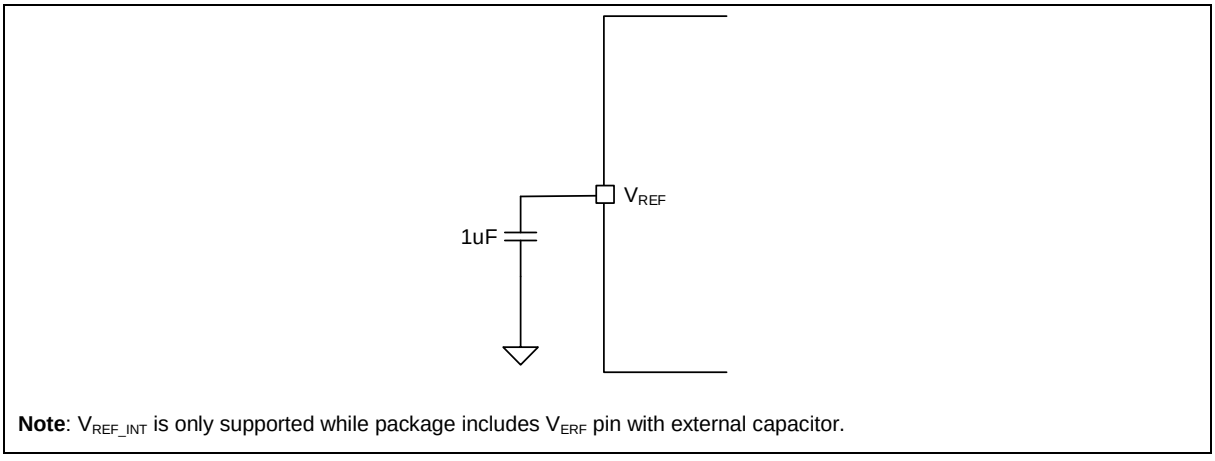
Figure 8.5-1 Power Ramp Up/Down Condition

8.5.4 Internal Voltage Reference

The maximum values are obtained for VDD = 3.6 V and maximum ambient temperature (TA), and the typical values for TA= 25 °C and VDD = 3.3 V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{REF_INT}	Internal reference voltage	-	1.6	-	V	AV_{DD} > 2.0v
		-	2.0	-		AV_{DD} > 2.2v
		-	2.5	-		AV_{DD} > 2.7v
		-	3.0	-		AV_{DD} > 3.2v
T_s	stable time	-		2	ms	C_L =4.7 uF, V_{REF} initial=0
		-		48	us	C_L =0.1 uF, V_{REF} initial=0
Note: Guaranteed by characterization, not tested in production.						

Table 8.5-4 Internal Voltage Reference



Note: V_{REF_INT} is only supported while package includes V_{ERF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.5 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	450	-	490	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 80 MHz $T_{CONV} = 14 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	0.14	-	80	MHz	High Speed Channel
T_{SMP}	Sampling Time	2	-	257	$1/F_{ADC}$	
T_{CONV}	Conversion time	14	-	269	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 14 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	-	-	5.71	MSPS	High Speed Channel $F_{SPS} = F_{ADC} / T_{CONV}$
INL[*1]	Integral Non-Linearity Error	-4.42	-	9.89	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	1.81	-	9.31	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	0.75	-	2.25	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-0.12	-	1.69	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	8.25	-	10.48	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	9.8	-	bits	F_{ADC} = 80 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	67	-	dB	
SNR[*1]	Signal-to-noise ratio	-	67	-		
THD[*1]	Total harmonic distortion	-	-72	-		
C_{IN}[*1]	Internal Capacitance	-	5	-	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Notes: 1. Guaranteed by characterization result, not tested in production. 2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy. $$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$						

Table 8.5-5 12-bit SAR Analog To Digital Converter

Low Speed Channel

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC1}	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	230	-	250	uA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 30 MHz low speed channel
		150	-	170		$AV_{DD} = V_{DD} = V_{REF}$ = 1.7V ADC Clock Rate = 30 MHz low speed channel
I_{ADC2}		112	-	119	uA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 14 MHz low speed channel
		72	-	75		$AV_{DD} = V_{DD} = V_{REF}$ = 1.7V ADC Clock Rate = 14 MHz low speed channel
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	0.14	-	30	MHz	Low Speed Channel
T_{SMP}	Sampling Time	2		257	$1/F_{ADC}$	
T_{CONV}	Conversion time	14		269	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 14 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	-	-	2.14	MSPS	Low Speed Channel $F_{SPS} = F_{ADC} / T_{CONV}$
INL[*1]	Integral Non-Linearity Error	-1.79		0.96	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	2.12	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	0.19	-	2.37	LSB	$V_{REF} = AV_{DD}$

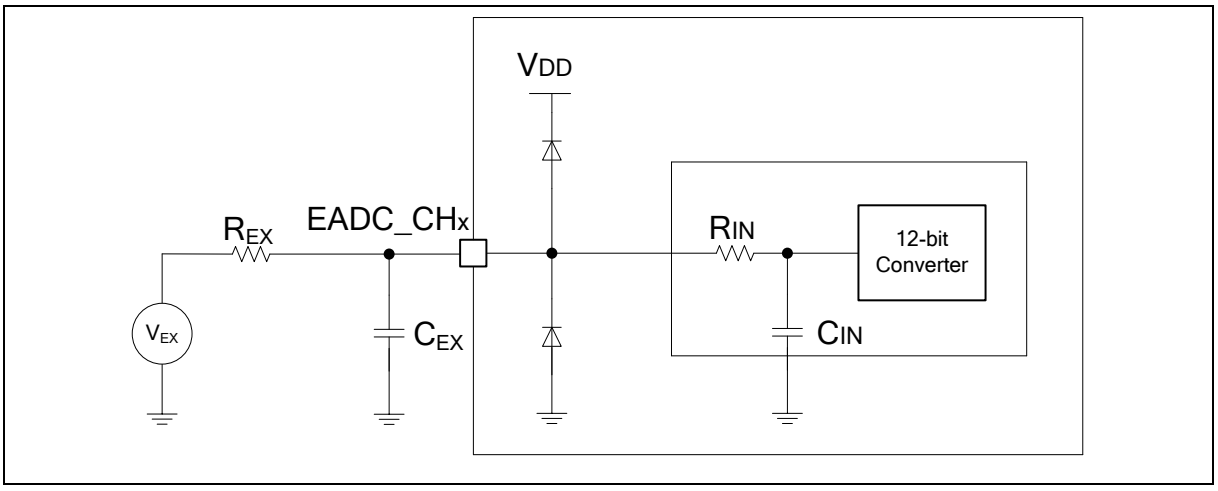
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
E_O[*1]$_T$	Offset error	-0.12	-	2.12	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	2.94	-	7.69	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	10.2	-	bits	F_{ADC} = 30 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	67	-	dB	
SNR[*1]	Signal-to-noise ratio	-	67	-		
THD[*1]	Total harmonic distortion	-	-72	-		
C_{IN}[*1]	Internal Capacitance	-	5	-	pF	

Notes:

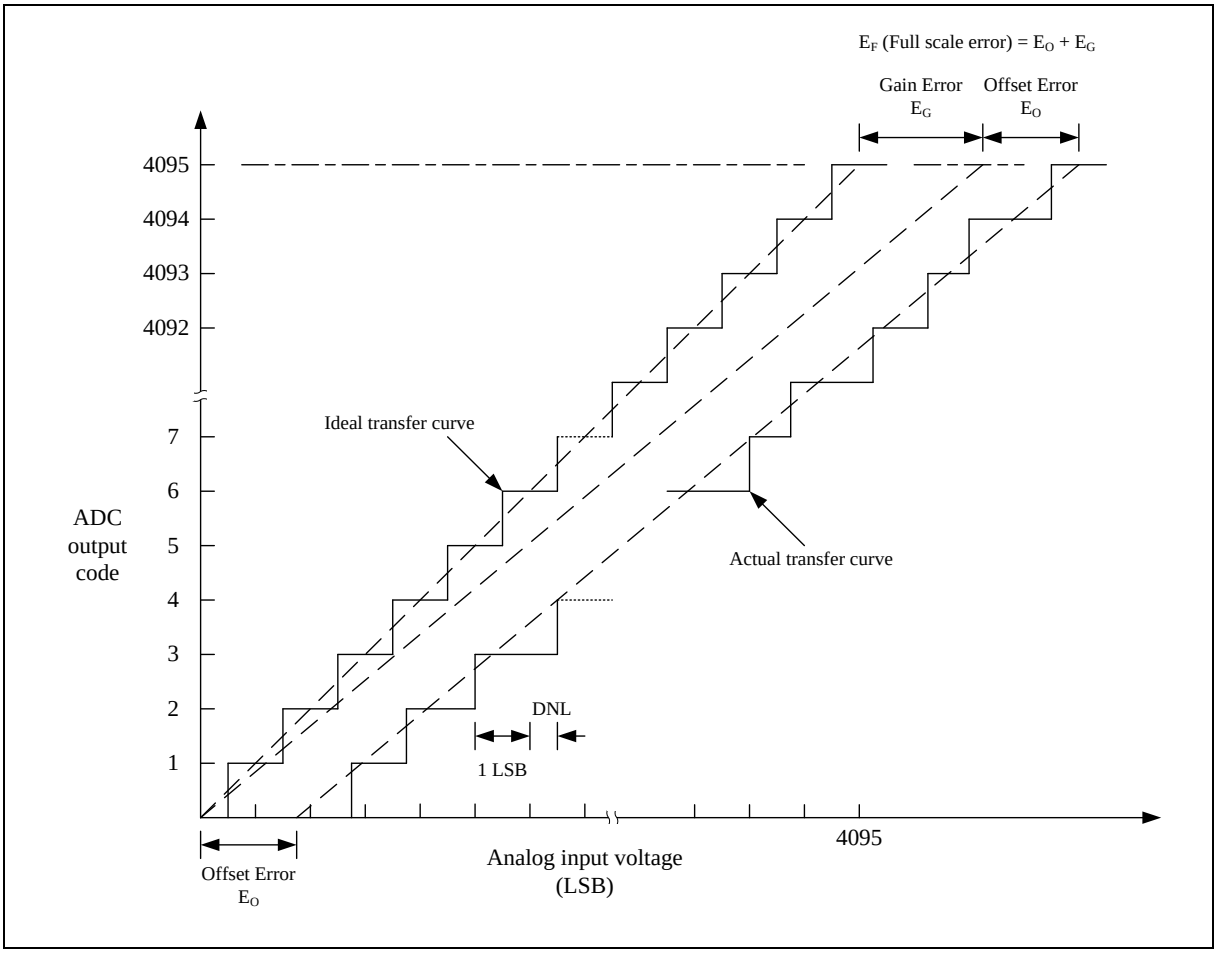
1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$

Table 8.5-6 12-bit SAR Analog To Digital Converter-low Speed



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.6 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	-
N_R	Resolution		12		bit	-
V_{REF}	Reference supply voltage	1.5	-	3.6	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error	-2	-	2	LSB	12-bit mode
		-0.5	-	-0.5	LSB	10-bit mode
INL[*2]	Integral non-linearity error	-4	-	4	LSB	12-bit mode
		-1	-	-1	LSB	10-bit mode
OE[*2]	Offset Error	-8	-	8	LSB	12-bit mode

						DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
		-2	-	-2	LSB	10-bit mode
$GE^{[*2]}$	Gain Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
		-2	-	-2	LSB	10-bit mode
$AE^{[*2]}$	Absolute Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
		-2	-	-2	LSB	10-bit mode
-	Monotonic	10-bit guaranteed			-	-
$V_O^{[*1]}$	Output Voltage	0.2	-	AVDD-0.2	V	DACOUT buffer ON
		1 LSB	-	V_{REF} – 1 LSB		DACOUT buffer OFF
$R_{LOAD}^{[*2][*3]}$	Resistive load	7.5	-	-	kΩ	DACOUT buffer ON
$R_O^{[*2]}$	Output impedance	-	9.8	-	kΩ	DACOUT buffer OFF
$C_{LOAD}^{[*2][*4]}$	Capacitive load	-	-	20	pF	DACOUT buffer OFF
$I_{DAC\_AVDD}^{[*2]}$	DAC operating current on AV_{DD} supply	-	132	-	µA	AV_{DD} = 3.6V, no load, lowest code (0x000)
		-	338	-		AV_{DD} = 3.6V, no load, middle code (0x800)
$I_{DAC\_VREF}^{[*2]}$	DAC operating current on V_{REF} supply	-	130	140	µA	V_{REF} =3.6V, no load, middle code (0x800)
$T_B^{[*2]}$	Settling Time	-	5	6	µs	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$
F_S	Update Rate	-	-	1	M_{SPS}	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$

T_{WAKEUP}	Wake-up Time	-	5	10	μs	Wakeup time from OFF state. Input code between lowest and highest possible codes. DAC clock source = 1MHz
PSRR[*1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

Table 8.5-7 Digital to Analog Converter

8.5.7 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	3.3	3.6	V	V_{DD} = AV_{DD}
T_A	Temperature	-40	-	125	℃	
I_{ACMP}[*2]	ACMP operating current	-	75	-	μA	MODESEL = 11
		-	10	-		MODESEL = 10
		-	3	-		MODESEL = 01
		-	1.2	-		MODESEL = 00
V_{CM}[*2]	Input common mode voltage range	0.1	1/2 AV_{DD}	AV_{DD} -0.1		
V_{DI}[*2]	Differential input voltage sensitivity	10	20	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	5	10	mV	Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	10	-	mV	HYSSEL = 01
		-	20	-		HYSSEL = 10
		-	30	-		HYSSEL = 11
A_v[*1]	DC voltage Gain	-	70	-	dB	
T_d[*2]	Propagation delay	-	-	4500	ns	Hysteresis disable MODESEL[1:0] = 00
		-	-	2000		Hysteresis disable MODESEL[1:0] = 01
		-	-	600		Hysteresis disable MODESEL[1:0] = 10
		-	-	200		Hysteresis disable MODESEL[1:0] = 11
T_{Setup}[*2]	Setup time	-	-	4750	ns	Hysteresis disable MODESEL[1:0] = 00
		-	-	2250		Hysteresis disable

						MODESEL[1:0] = 01
		-	-	850		Hysteresis disable MODESEL[1:0] = 10
		-	-	450		Hysteresis disable MODESEL[1:0] = 11
A_{CRV}[*2]	CRV output voltage	-5%	-	+5%	%	AV_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.2k	-	kΩ	
I_{DD_CRV}[*2]	Operating current	-	32.7	-	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-8 Analog Comparator Controller

8.5.8 Temperature Sensor

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Tempereture sensor offset voltage	710	720	730	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	-1.77	-1.82	-1.86	mV/°C	
T_S[*2]	Stable time	-	3	-	μS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	-	3	-	μS	
I_{TEMP}[*1]	OPA operating current	-	16	-	μA	

Note:

8.1.4.3.1.1 Guaranteed by characterization, not tested in production

8.1.4.3.1.2 Guaranteed by design, not tested in production

8.1.4.3.1.3 V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Table 8.5-9 Temprature Sensor

8.5.9 LCD controller

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Supply voltage	1.6	-	3.6	V	
T_A	Temperature	-20	-	85	℃	
V_{LCD}	LCD external voltage	2.6	-	3.6	V	
	LCD internal voltage	2.5	2.6	2.7		VSEL = 0 @ V_{DD} = 1.8V
		2.7	2.8	2.9		VSEL = 1 @ V_{DD} = 1.8V

		2.9	3	3.1		VSEL = 2 @ V_{DD} = 1.8V
		3.1	3.2	3.3		VSEL = 3 @ V_{DD} = 1.8V
		3.3	3.4	3.5		VSEL = 4 @ V_{DD} = 1.8V
		3.5	3.6	3.7		VSEL = 5 @ V_{DD} = 1.8V
C_{LCD}	V_{LCD} external capacitance	-	1	2	μF	BUFEN = 0 Without buffer mode
		-	1	2		BUFEN = 1 With buffer mode
I_{LCD}[*2]	Supply current from V_{DD} with built-in charge pump and buffer mode	-	124.4	-	μA	VSRC = 2, BUFEN = 0, V_{LCD} = 2.6V, V_{DD} = 1.6V
		-	150.1	-		VSRC = 2, BUFEN = 0, V_{LCD} = 3.6V, V_{DD} = 3.6V
		-	104.1	-		VSRC = 2, BUFEN = 1, V_{LCD} = 2.6V, V_{DD} = 1.6V
		-	126.4	-		VSRC = 2, BUFEN = 1, V_{LCD} = 3.6V, V_{DD} = 3.6V
I_{VLCD}[*2]	Supply current from V_{LCD} without Bulit-In Charge Pump	-	3.3	-	μA	VSRC = 0, BUFEN = 1, V_{LCD} = 2.6V, buffer mode
		-	4.3	-		VSRC = 0, BUFEN = 1, V_{LCD} = 3.6V, buffer mode
		-	2.13	-		VSRC = 0, RES_MODE = 1, V_{LCD} = 2.6V, low drive mode
		-	2.64	-		VSRC = 0, RES_MODE = 1, V_{LCD} = 3.6V, low drive mode
		-	13	-		VSRC = 0, RES_MODE = 1, V_{LCD} = 2.6V, high drive mode
		-	17.5	-		VSRC = 0, RES_MODE = 1, V_{LCD} = 3.6V, high drive mode
R_{LCD_INT}	Internal total LCD resistor value	-	5.5	-	MΩ	Low drive
		-	240	-	kΩ	High drive

Note:

1. Guaranteed by design, not tested in production
2. LCD COM/SEG is set to 1/8 duty, 1/4 bias, 30 Hz frame rate, all pixels active, type B waveform, no LCD panel loading.

Table 8.5-10 LCD Controller

8.6 Commucications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
SPI Master Mode (V_{DD} = 3.0~3.6 V, 30 PF loading Capacitor)					
t_{CLKL}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKH}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	10	-	-	ns
t_V	Data output valid time	-	0	15	ns

Table 8.6-1 SPI Master Mode Characteristics

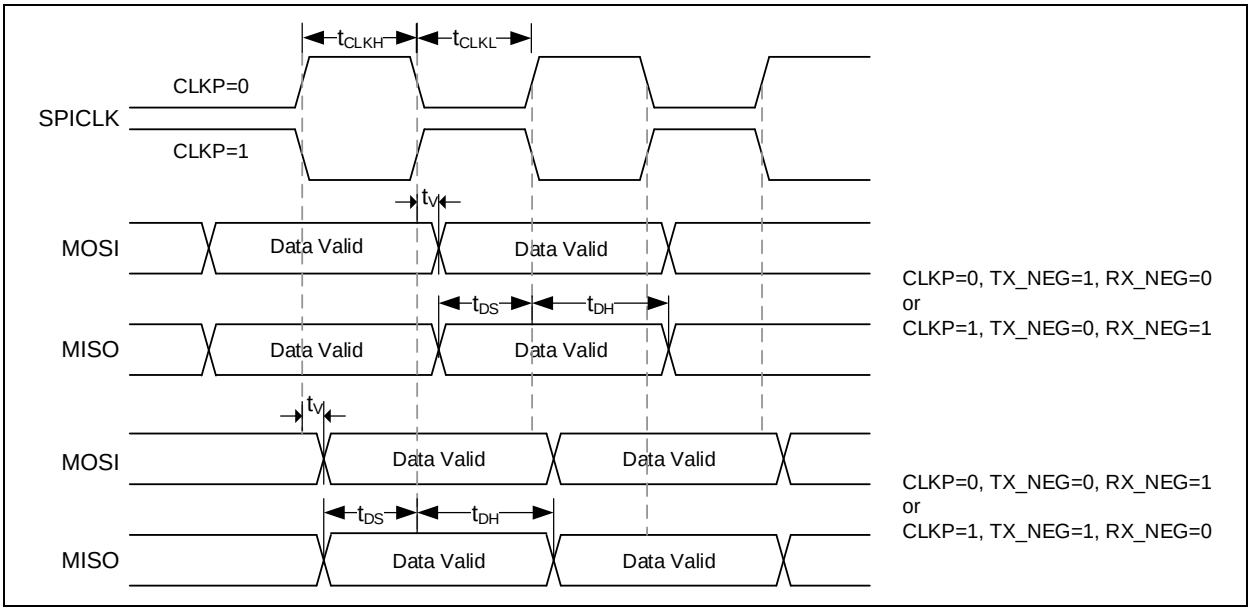


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
SPI Slave Mode (V_{DD} = 3.0~3.6V, 30 PF Loading Capacitor)					
t_{CLKL}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	Peripheral clock
t_{CLKH}	Clock output Low time [*1]	-		T_{SPICLK} / 2	Peripheral clock
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	Peripheral clock
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	Peripheral clock
t_{DS}	Data input setup time	0	-	-	ns

t_{DH}	Data input hold time	6	-	-	ns
t_V	Data output valid time	-	-	11.5	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns

Note: The minimum clock period for SPICLK is 41.67 ns (24 MHz).

Table 8.6-2 SPI Slave Mode Characteristics

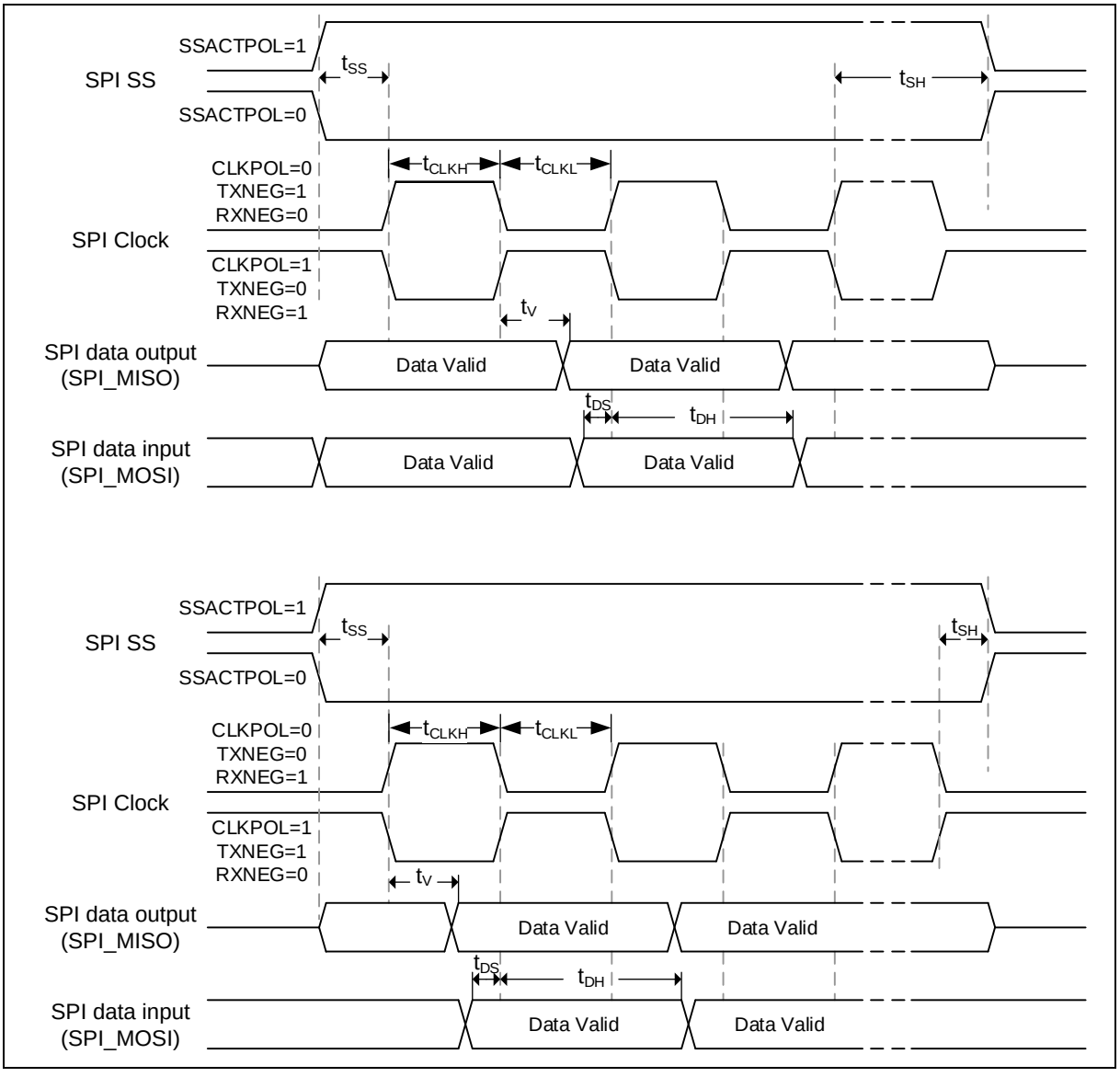


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I^2S clock high time	39	-	ns	Master fPCLK = MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I^2S clock low time	39	-		
$t_{v(WS)}$	WS valid time	2	12		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I^2S slave input clock duty cycle	35	65	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	22	-	ns	Master receiver
$t_{su(SD\_SR)}$		10	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		8	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	21		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	7		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I^2S Characteristics

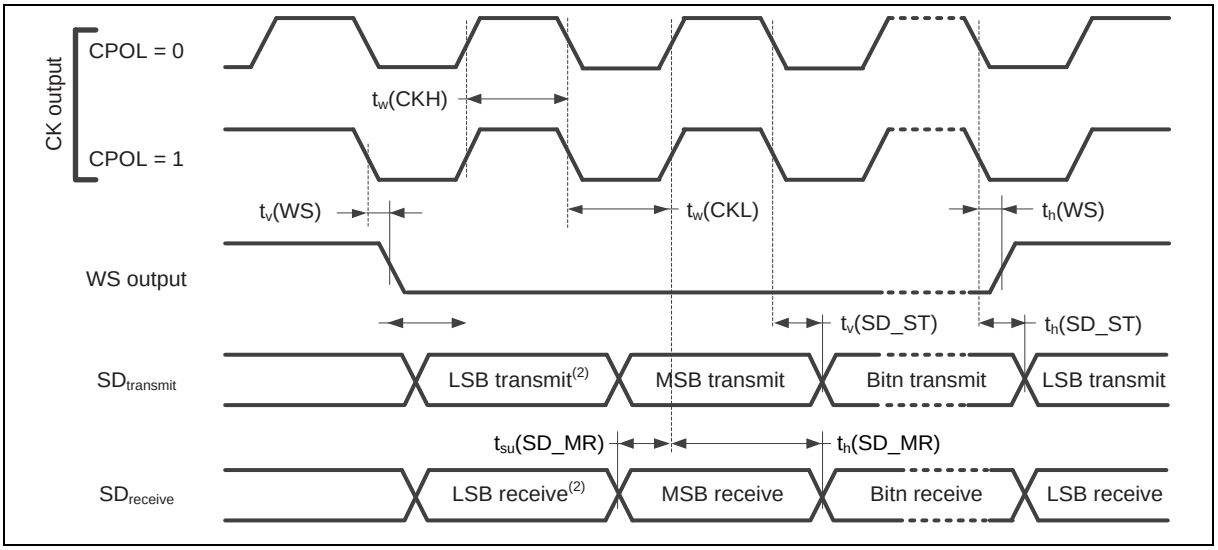


Figure 8.6-3 I^2S Master Mode Timing Diagram

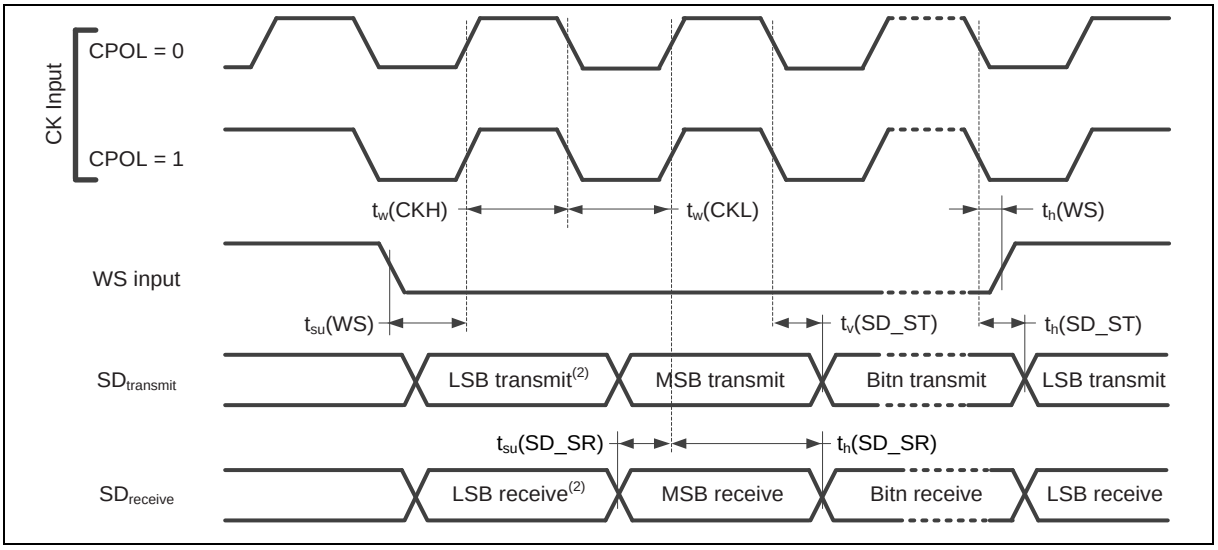


Figure 8.6-4 I^{2}S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.2	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7 [3]	-	1.2 [3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0 [4]	3.45 [5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1 C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

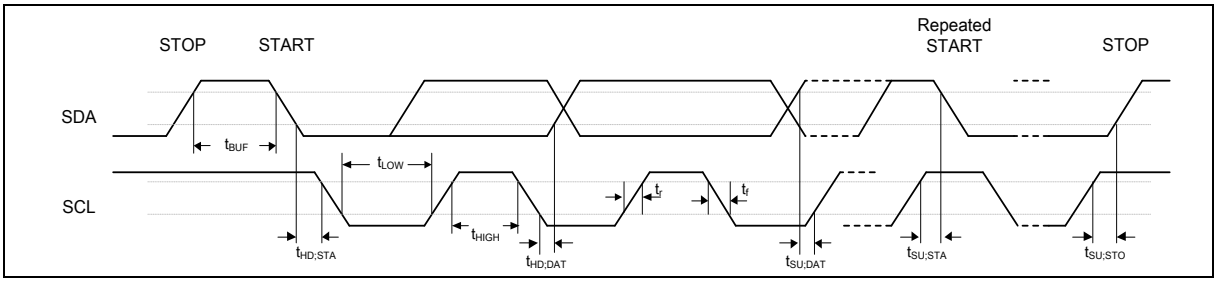


Figure 8.6-5 I²C Timing Diagram

8.6.4 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
SPI Master Mode (V_{DD} = 3.0~3.6 V, 30 PF loading Capacitor)					
t_{CLKL}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKH}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns

Table 8.6-5 USCI-SPI Master Mode Characteristics

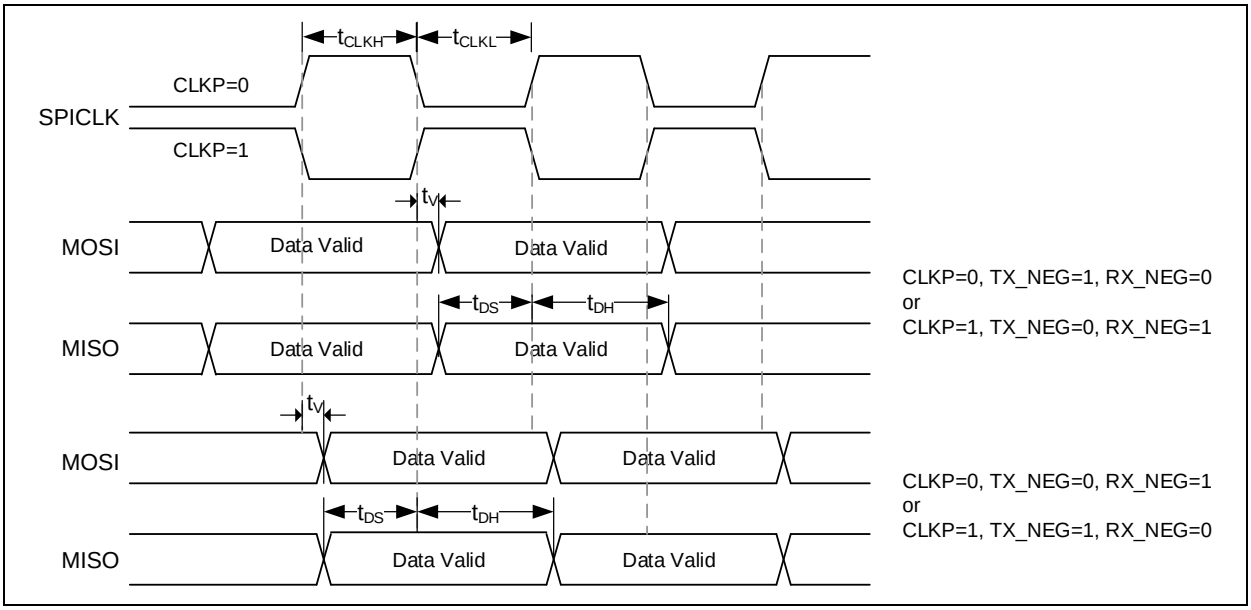


Figure 8.6-6 USCI-SPI Master Mode Timing Diagram

8.6.5 USCI - I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.2	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7 [3]	-	1.2 [3]	-	µs

$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0 [4]	3.45 [5]	0 [4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1 C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-6 USCI-I^2C Characteristics

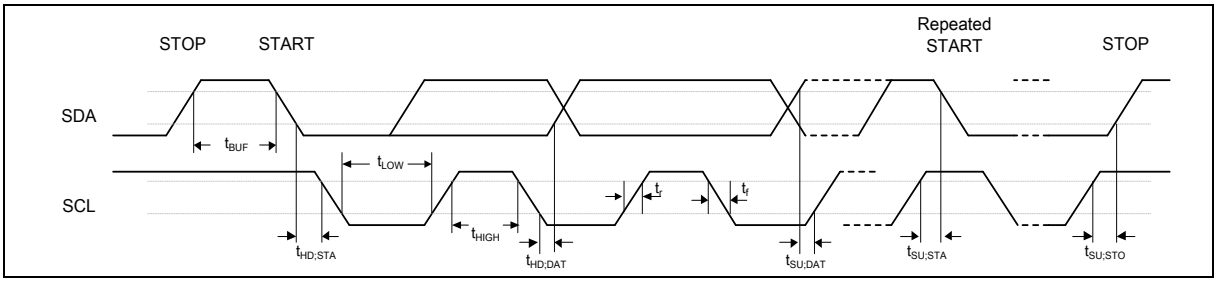


Figure 8.6-7 USCI-I^2C Timing Diagram

8.6.6 USB Characteristics

8.6.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	-	0.2	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
R_{PD}	Pull-down Resistor	14.25	-	24.8	kΩ	

R_{PU}	Pull-up resistor	1.425	-	3.09	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV} [*2]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Notes:

1. Guaranteed by characterization result, not tested in production.
2. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-7 USB Full-Speed Characteristics

8.6.6.2 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	ns	C_L=50 pF
T_{FF}	fall time	4	-	20	ns	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-8 USB Full-Speed PHY Characteristics

8.6.7 SDIO Characteristics

Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Table 8.6-9 SDIO Characteristics

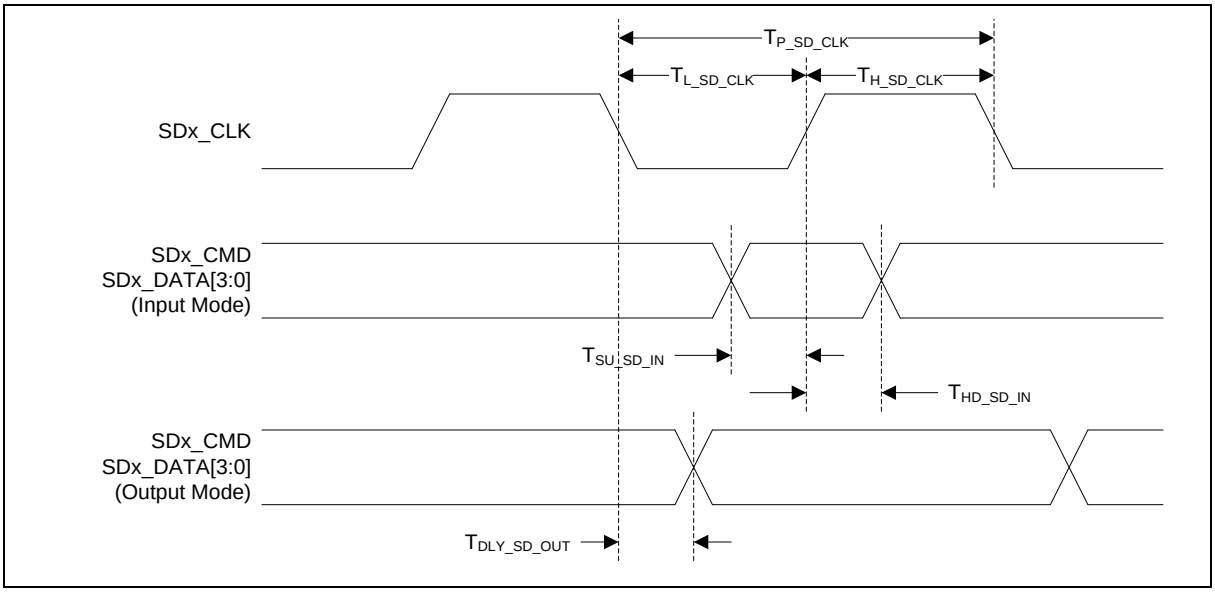


Figure 8.6-8 SDIO Default Mode

SDIO Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Table 8.6-10 SDIO Dynamic Characteristics

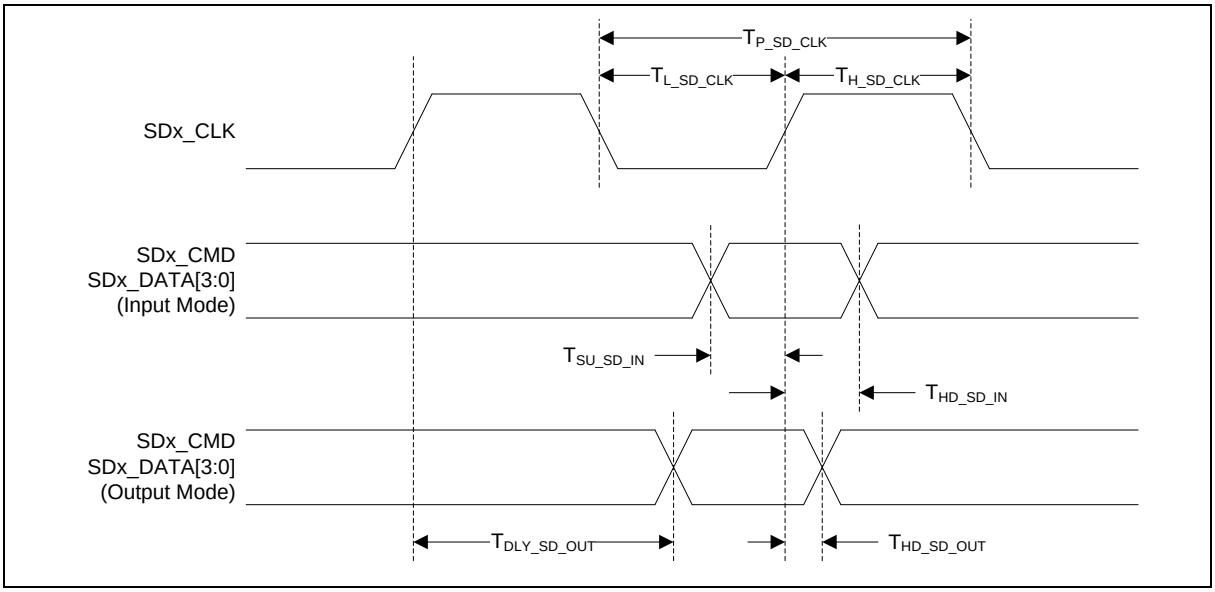


Figure 8.6-9 SDIO High-speed Mode

8.7 Flash DC Eletrical Charateristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	0.81	1.2	1.32	V	T_A = 25℃
T_{ERASE}	Page erase time	93		160	ms	
T_{PROG}	Program time	1237	-	1800	µs	
I_{DD1}	Read current	42		50	mA	
I_{DD2}	Program current	-		4.12	mA	
I_{DD3}	Erase current	-		5	mA	
N_{ENDUR}	Endurance	-		5	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	10000	-		year	20 kcycle[3] T_J = 55℃
		-	-	-	year	20 kcycle[3] T_J = 85℃
		10	-	-	year	20 kcycle[3] T_J = 125℃

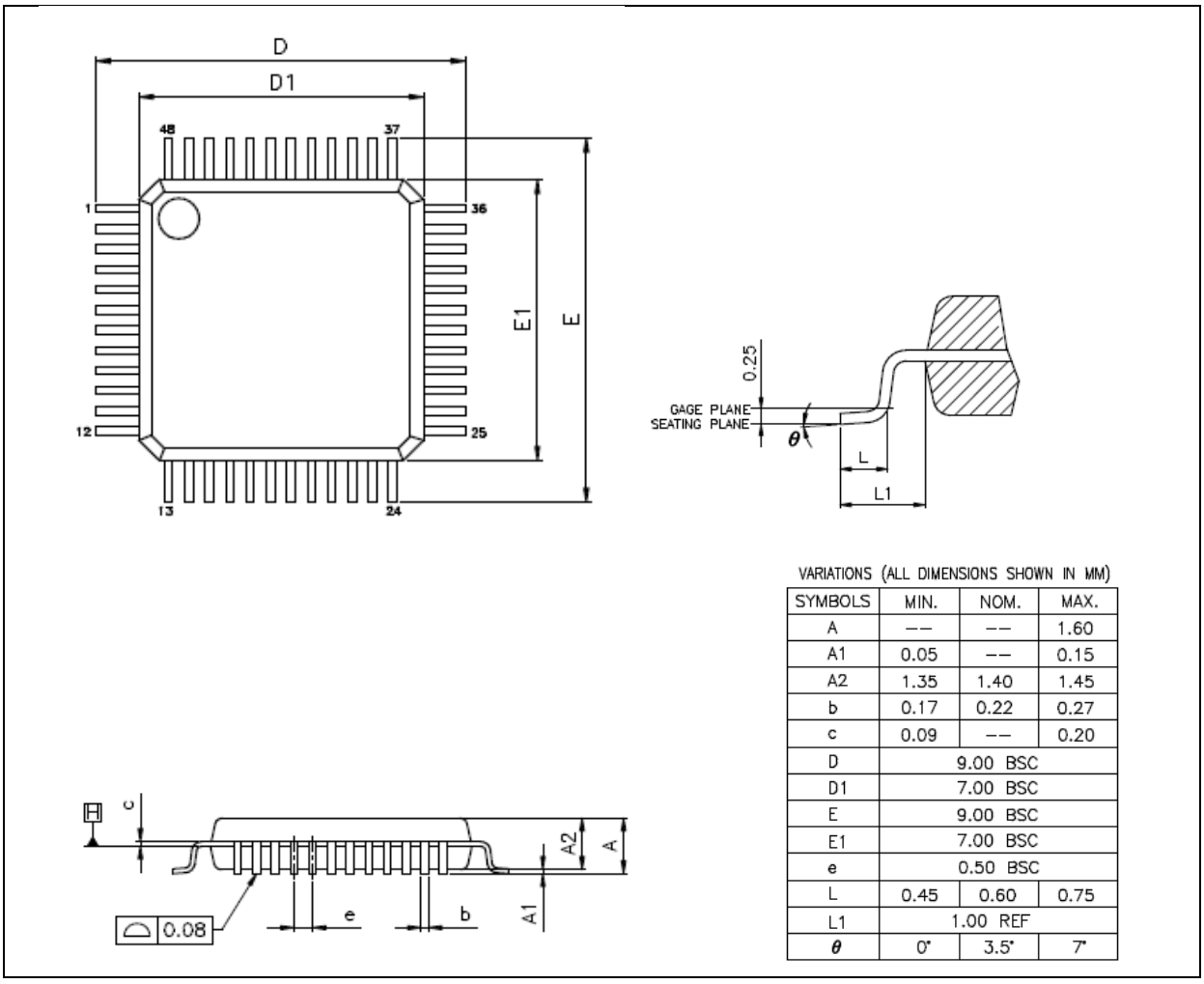
Notes:

1. V_{FLA} is source from chip internal LDO output voltage, and the Flash memoy can support just read operation when V_{FLA} < 1.08V
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.7-1 Flash DC Eletrical Characteristics

9 PACKAGE DIMENSIONS

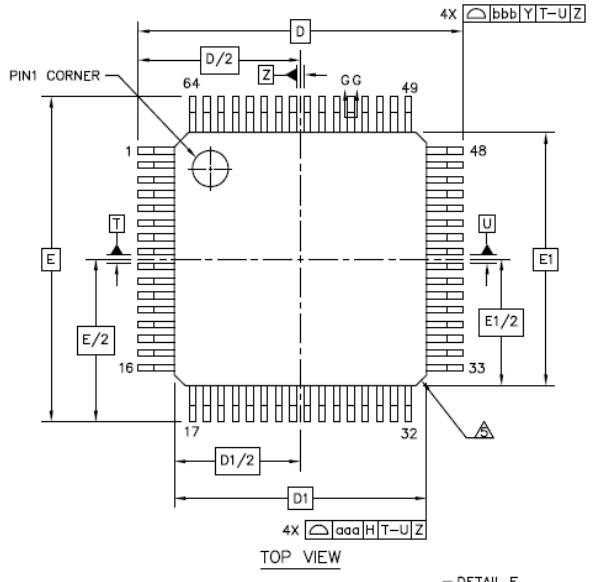
9.1 LQFP 48 (7x7x1.4 mm^3 Footprint 2.0 mm)

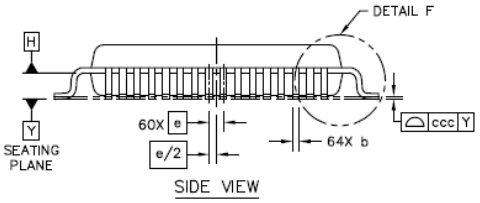


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

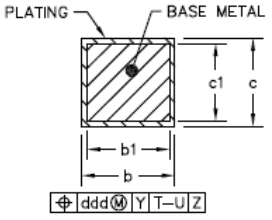
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

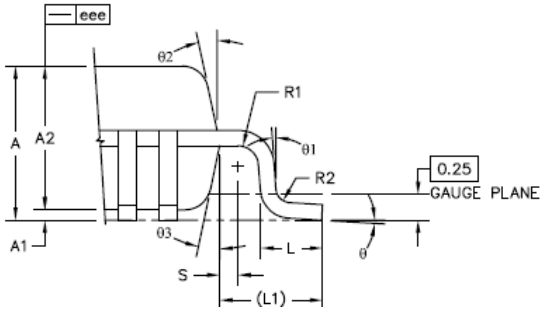
9.2 LQFP 64 (7x7x1.4 mm^3 Footprint 2.0 mm)



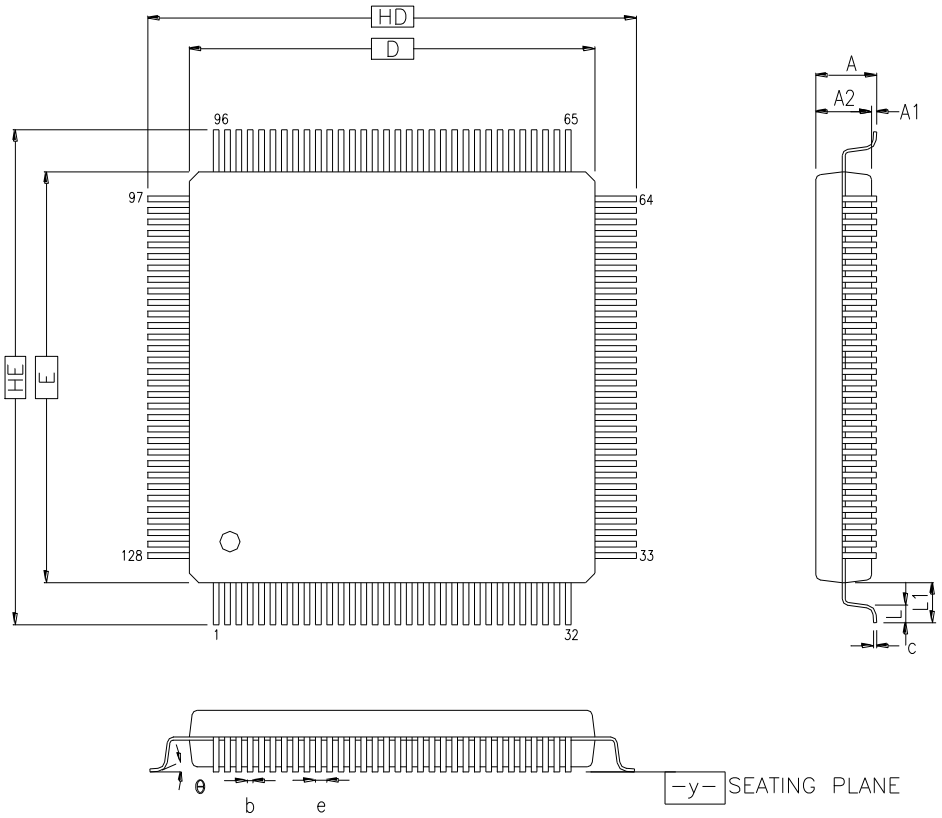


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





9.3 LQFP 128 (14x14x1.4 mm^3 Footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop

PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2020.12.25	1.00	Initial version.
2021.07.30	1.01	1. Added internal reference voltage function in chapter 2 and section 6.37.2, 6.42.2 and 8.5.4. 2. Removed V_{DDIO} constraint in section 8.2. 3. Revised I_{LCD} and I_{VLCD} in section 8.5.9 4. Revised Max value on Power-down mode in section 8.3.1.5

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.