FSC-BT646

BLE 4.2 Single Mode Bluetooth Module Datasheet

Version 2.6

Revision History

Version	Data	Notes	
2.0	2018/12/04	Initial Version	Fish
2.1	2018/12/18	Upgrade to BLE 4.2	Fish
2.2	2019/08/06	Update sleep mode power consumption, supply voltage range	Fish
2.3	2019/08/29	Increase the certification directory	Fish
2.4	2019/10/10	Increase the certification directory(FCC、CE、BQB)	Fish
2.5	2019/10/18	Feature update	Fish
2.6	2020/04/30	Increase power consumption parameters	Fish

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Contents

1. INTRODUCTION

Overview

FSC-BT646 is Bluetooth Low Energy 4.2(BLE4.2) Module. It can be used as an application processor as well as a data pump in fully hosted systems. MCU is 32-bit microcontroller. It supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

Very low active RF, MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

The BLE4.2 firmware includes the L2CAP service layer protocols, Security Manager (SM), At-tribute Protocol (ATT), the Generic Attribute Profile (GATT) and the Generic Access Profile (GAP).

Features

- 2.4-GHz RF Transceiver Compatible With Bluetooth low energy (BLE) 4.2
- Programmable TX power up to 13dBm(Class 1)
- RX sensitivity up to -90dBm
- Postage stamp sized form factor
- Programmable baud-rate generator(baudrate can up to 921600bps)
- UART, I2C,SPI,12-bit ADC,PWM connection interfaces
- Bluetooth stack profiles support: HID
- Operating Voltage:2.2V to 3.6V
- Operating Temperature: -40°C to +85°C
- SRRC, FCC, CE and BQB Certified
- Power Consumption In Sleep Mode (VDD_3V3 at 3.3V)
  - Discoverable：503.72uA
  - LE Connection：586.52uA
- Power Consumption In Working Mode (VDD_3V3 at 3.3 V)
  - Discoverable：6.05mA
  - LE Connection：6.24mA
  - LE Connection @ 115200bps：6.32mA

Application

- Health Thermometer
- Heart Rate
- Blood Pressure
- Proximity
- Human Interface Device (HID)

Module picture as below showing

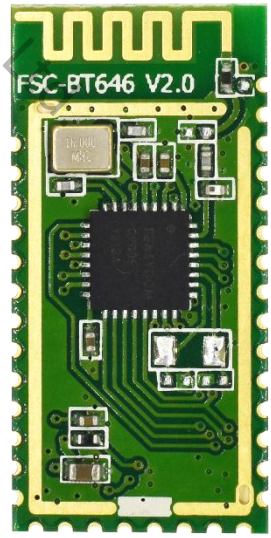


Figure 1: FSC-BT646 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	Bluetooth low energy 4.2
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+13 dBm (Maximum)
	Receive Sensitivity	-90 dBm (Typical)
	Modulation	GFSK
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	22(maximum – configurable) lines
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	2(configurable from GPIO total). Up to 400 kbps
	ADC Interface	Analog input voltage range: 0.4V ~ 1.4V(or 2.4V) based on configure
		Supports single 12-bit SAR ADC conversion
		8 channels (configured from GPIO total)
		Up to 200MSPS conversion
	PWM	8 PWM outputs
		Supports edge-alignment or center-alignment Supports fault detection
Profiles	Class Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
Maximum Connections	Classic Bluetooth	No Support
FW upgrade		J-Link
Supply Voltage	Supply	2.2V ~ 3.6V
Power Consumption		Deep Sleep - 8uA(Wake up by wakeup PAD or RESET)
Physical	Dimensions	13mm X 26.9mm X 2.0mm; Pad Pitch 1.5mm
Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +125°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model	All pins: ±4000V
	Charged device model	RF pins/ Non-RF pins: ±750V

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

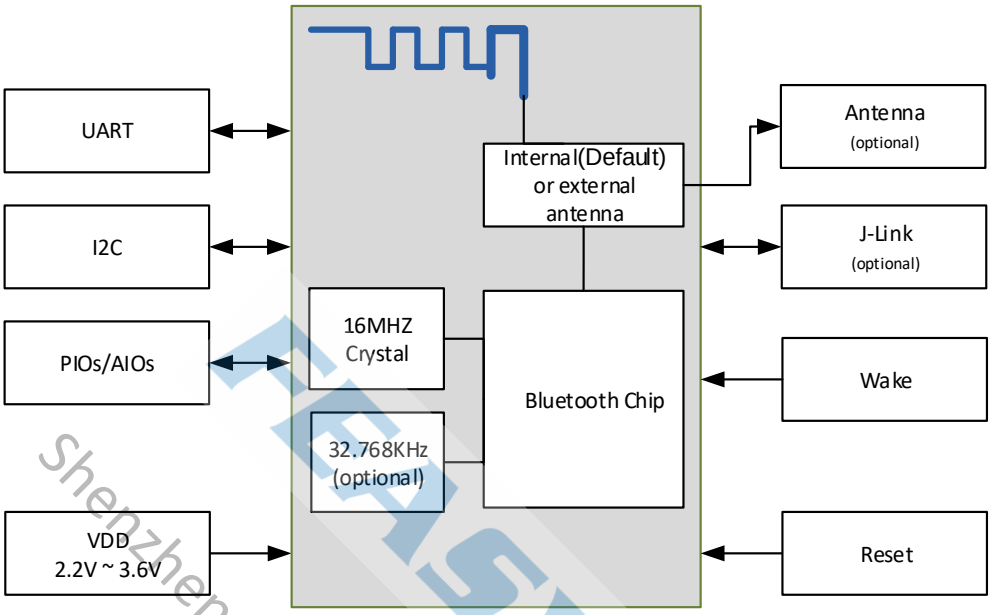


Figure 2: Block Diagram

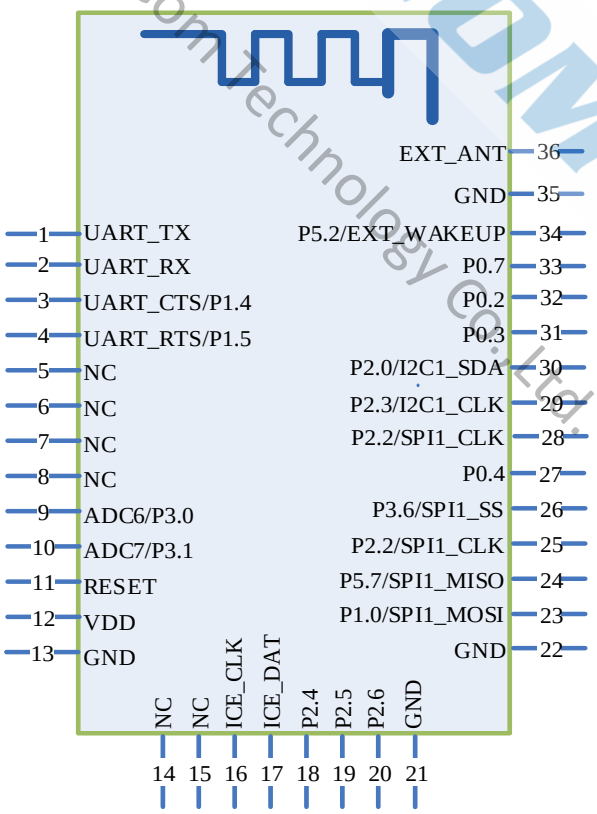


Figure 3: FSC-BT646 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART data output	Note 1
2	UART_RX	I	UART data input	Note 1
3	UART_CTS/P1.4	I	UART clear to send active low Alternative Function: Programmable input/output line	Note 1
4	UART_RTS/P1.5	I/O	UART request to send active low Alternative Function: Programmable input/output line	Note 1
5	NC		NC	
6	NC		NC	
7	NC		NC	
8	NC		NC	
9	ADC6/P3.0	I/O	Programmable input/output line Alternative Function: Analogue programmable I/O line	Note 1
10	ADC7/P3.1	I/O	Programmable input/output line Alternative Function: Analogue programmable I/O line	Note 1
11	RESET	I	External reset input: Active LOW, with an inter an internal pull-up Set this pin low reset to initial state	
12	VDD	Vdd	Power supply voltage 2.2V ~ 3.6V	
13	GND	Vss	Power Ground	
14	NC		NC	
15	NC		NC	
16	ICE_CLK	I/O	Debugging through the CLK line(Default)	Note 1
17	ICE_DAT	I/O	Debugging through the DATA line(Default)	Note 1
18	P2.4	I/O	Programmable input/output line	
19	P2.5	I/O	Programmable input/output line	
20	P2.6	I/O	Programmable input/output line	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	**P1.0/SPI1_MOSI**	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 6
24	**P5.7/SPI1_MISO**	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 6
25	**P2.2/SPI1_CLK**	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 6
26	**P3.6/SPI1_SS**	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 6
27	P0.4	I/O	Programmable input/output line	
28	**P2.2/SPI1_CLK**	I	Programmable input/output line *** The I/O port for reuse.**	Note 6
29	P2.3/I2C1_CLK	I/O	Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3

30	P2.0/I2C1_SDA	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
31	P0.3	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth	Note 1
32	P0.2	I/O	Programmable input/output line Alternative Function: LED(Default)	Note 1,4
33	P0.7	I/O	Programmable input/output line Alternative Function: BT Status(Default)	Note 1,2
34	P5.2/EXT_WAKEUP	I/O	Programmable input/output line	
35	GND	Vss	RF Ground	
36	EXT_ANT	O	RF signal output	Note 5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status (Default)-- Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.
Note 6	This I / O port is shared with the internal SPI Flash chip. We do not recommend using this pin, floating processing. This pin is only available when the module is not equipped with air-upgrade function.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

4.3 General Purpose Analog IO

- 12-bit resolution and 10-bit accuracy
- Analog input voltage range: 0.4~1.4 or 0.4~2.4V based on configure
- Up to eight single-end analog input channels
- Two operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - PWM sequence mode: When PWM trigger, two of three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0,1] or channel[1,2] or channel[0,2] defined by MODESEL (ADC_SEQCTL[3:2])
- An A/D conversion can be started by
  - Software write 1 to SWTRG bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each Conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 8 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

4.4 General Purpose Digital IO

There are 22 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 30 kΩ ~ 50 kΩ for VDD and Vss.

4.5 RF Interface

For This Module, the default mode for antenna is internal ,it also has the interface for external antenna. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz BLE4.2
- TX output power of +13dBm.
- RX sensitivity up to -90dBm

4.6 Serial Interfaces

4.6.1 UART

FSC-BT646 provides one channels of Universal Asynchronous Receiver/Transmitters (UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT646 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 3: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

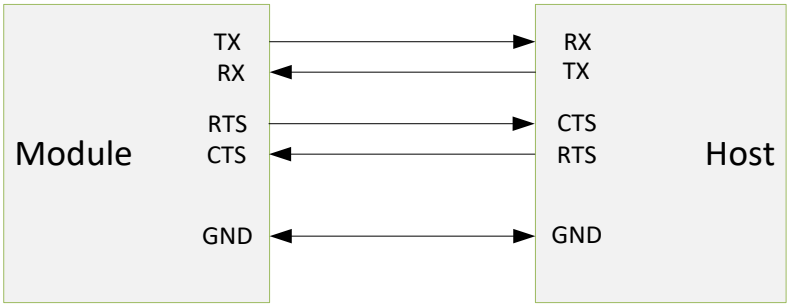


Figure 4: UART Connection

4.6.2 I²C Interface

- Two I2C master and slaver devices with DMA
- Bidirectional data transfer between masters and slaves
- Multi-master bus Arbitration between simultaneously transmitting masters without cor-ruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and re-sume serial transfer
- Built-in 14-bit time-out counter that requests the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition

4.7 PWM Interface

- Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four com-plementary paired PWM outputs
- Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
- PWM interrupt synchronized to PWM period
- Supports edge-alignment or center-alignment
- Supports fault detection

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Symbol	Description	Min	Trp	Max	Unit
VDD	BT Input voltage	-0.3	-	3.6	V
VI	Input voltage	-0.3	-	VDD	V
VO	Output voltage	VSS	-	VDD	V
TOP	Operating Temperature	-40	-	85	°C
TSTG	Storage Temperature	-40	-	125	°C

Note: Exceeding one or more of the limiting values may cause permanent damage to FSC-BT646.
Caution: Electrostatic sensitive device, comply with protection rules when operating.

5.2 DC Electrical Characteristics

Table 5: Voltage and current

Symbol	Parameter	Min	Type	Max	Unit	Test Conditions
V_{DD}-V_{SS} -	DC Power Supply	2.2	3	3.6	V	TA=25°C
T_A -	Operating Temperature	-40	25	+85	°C	-
I1	Standby Current in Sleep mode	-	8	-	uA	Wakeup PAD or RESET
VOH	Output high level voltage	VDD-0.3	-	VDD	V	-
VOL	Output low level voltage	VSS	-	VSS+0.3	V	-
VIH	Input high level voltage	2.0	3	3.6	V	-
VIL	Input low level voltage	VSS	-	VSS+0.3	V	-

5.3 AC Electrical Characteristics

Table 6: RF

Symbol	Parameter	Min	Type	Max	Unit
General frequency					
Fop	Operating frequency	2402	-	2480	MHz
PLLres	PLL Programming resolution	-	1	-	MHz
Fxtal	Crystal frequency	-	16	-	MHz
DR	Data rate	-	1	-	Mbps
△f1M	Frequency deviation	225	250	275	KHz
FCH1M	Channel spacing	-	2	-	MHz
Transmitter					
PRF	Output power	-18	-	13	dBm
PBW	20dB Bandwidth for Modulated Carrier at 1Mbps	-	1.5	-	MHz
Receiver					
RXmax	Maximum received signal at <0.1% BER	-	-10	-	dBm
RXSENS	Sensitivity (0.1%BER) @1Mbps	-	-90	-	dBm
C/ICO	C/I Co-channel interference	-	11	-	dB
C/I1MHz	Adjacent 1MHz interference	-	-2	-	dB
C/I2MHz	Adjacent 2MHz interference	-	-22	-	dB
C/I3MHz	Adjacent ≥3MHz interference	-	-38	-	dB
C/Iimage	Image frequency interference	-	-12	-	dB
C/ Iimage±1MHz	Ajacent 1MHz interference to in-band image freq	-	-24	-	dB

Table 7: ADC

Symbol	Parameter	Min	Type	Max	Unit
Resolution	-	-	12	-	Bit
Enob	-	-	10	-	Bit
IOT	Operation Current	880	1000	1660	uA

Pclk	System Clock	-	-	52	MHz
FS	Sample Rate	-	-	0.5	MHz
Fin	-	0	-	40	KHz
Vrefp-Vrefn	Analog input voltage, Reference voltage Vbg	1	2	2	V
Cin	Input Capacitane	-	10	-	pF
VCM	-	0.9	-	1.4	V
DATA	ADC Output	000	-	FFF	HEX
SFDR	Spurious Free Dynamic range	-	72	-	dB

6. MSL & ESD

Table 8: MSL and ESD

Parameter	Test Conditions		Value
MSL grade:	MSL 3(1)		
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(2)	All pins	±4000V
	Charged device model (CDM), per JESD22-C101(3)	RF pins	±750V
		Non-RF pins	±750V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 9: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%

3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

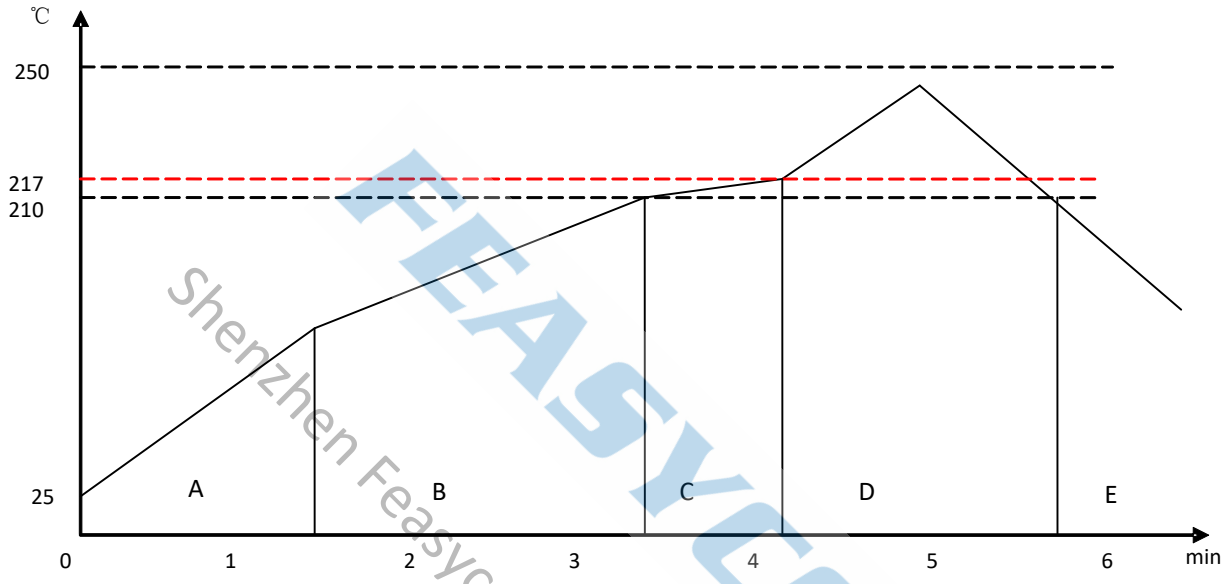


Figure 5: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0 mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

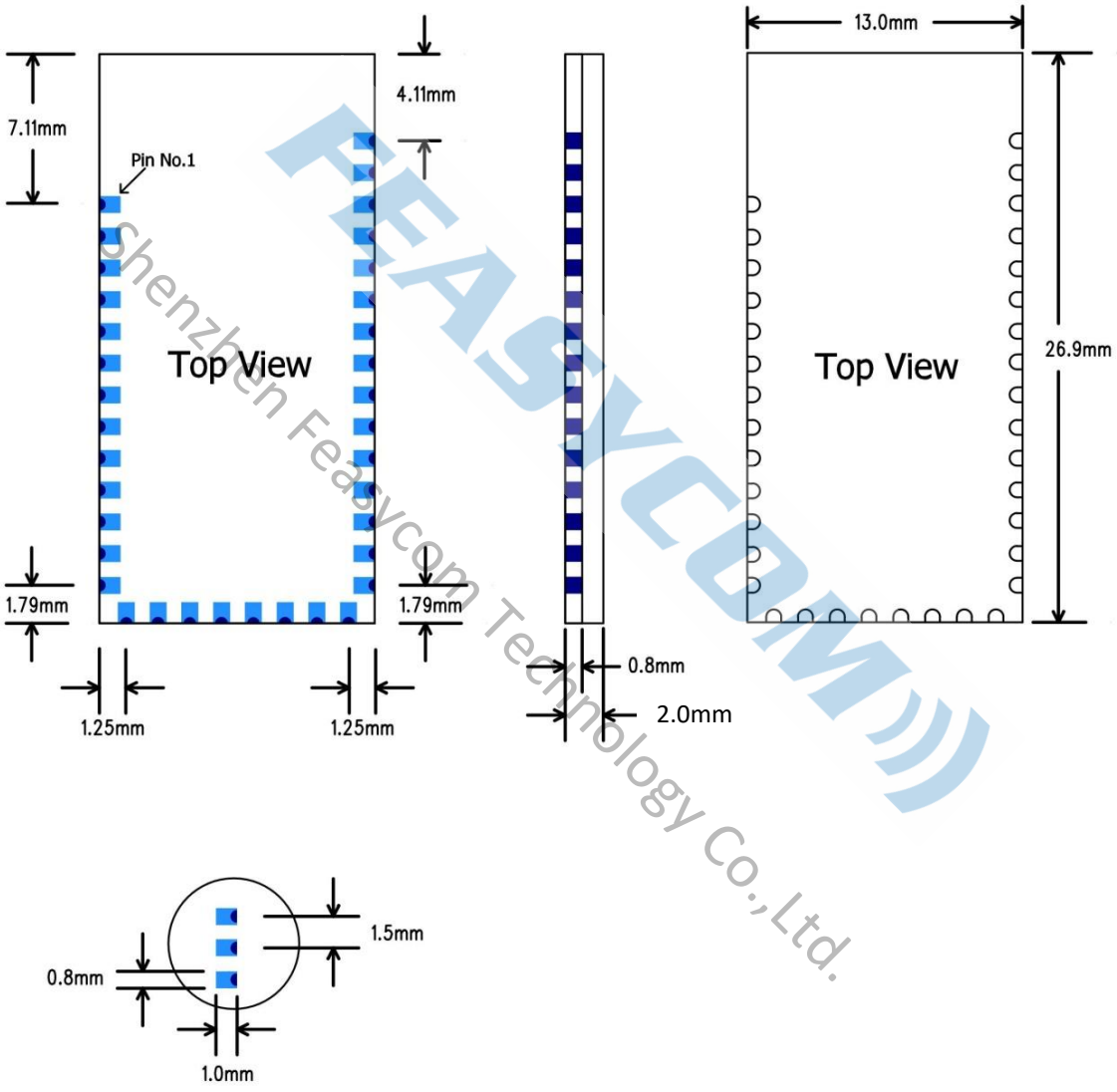


Figure 6: FSC-BT646 footprint

8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BT646

Please check the picture below for Pad Structure and Keep Out Area:

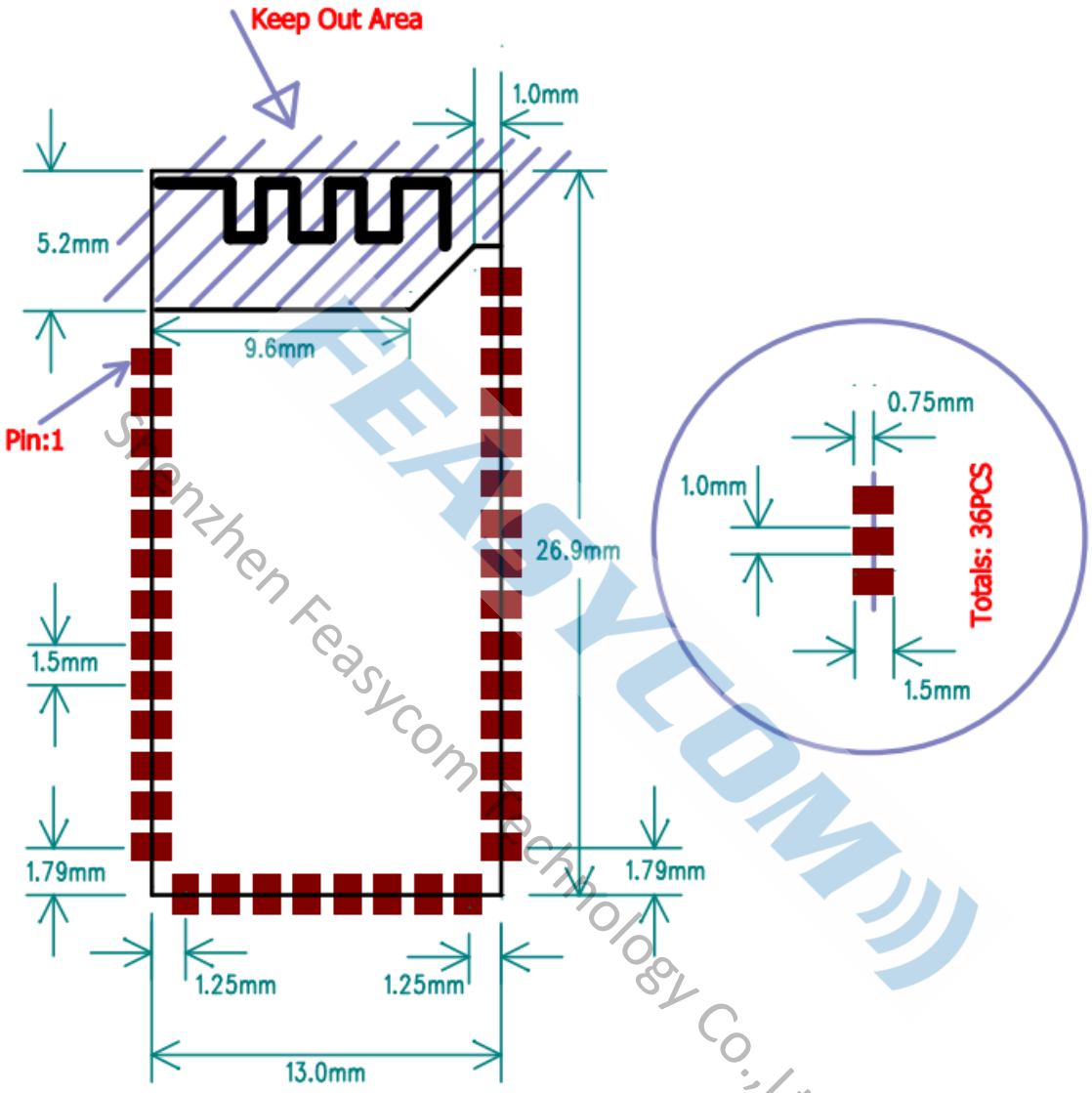


Figure 7: Host PCB-Top View

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT646 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

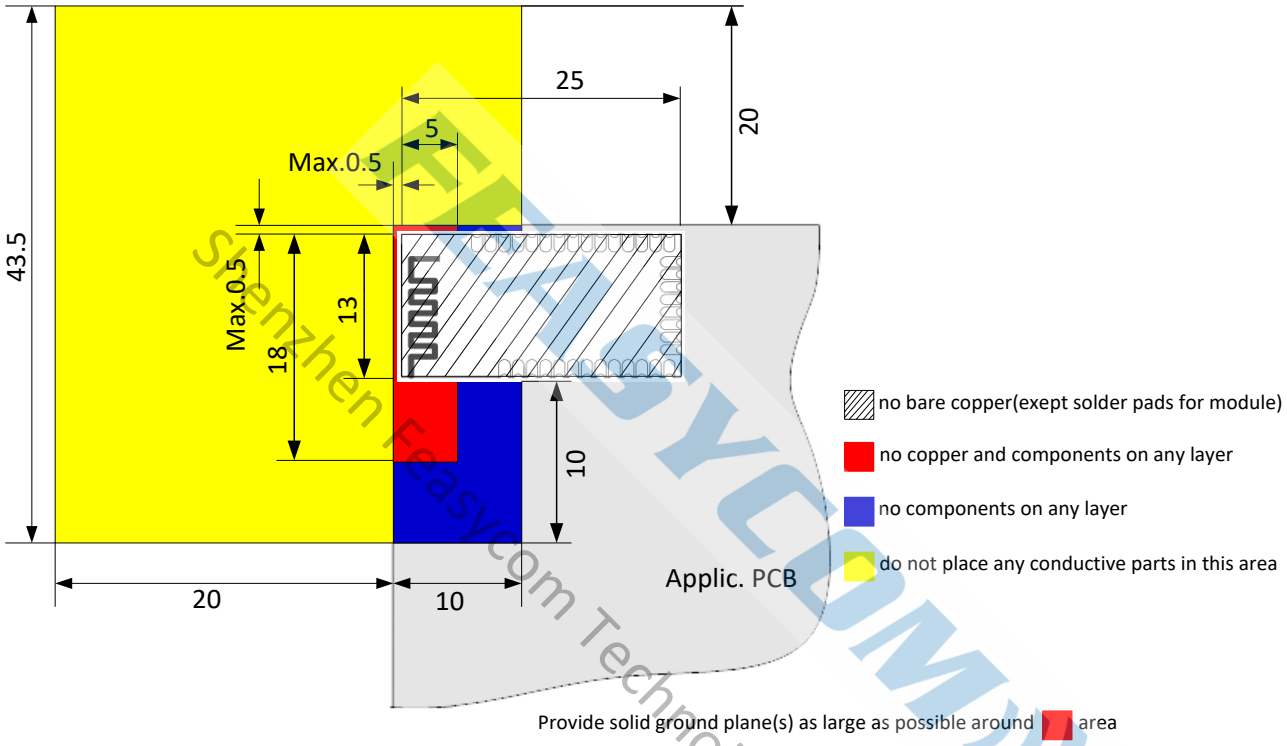


Figure 8: FSC-BT646 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

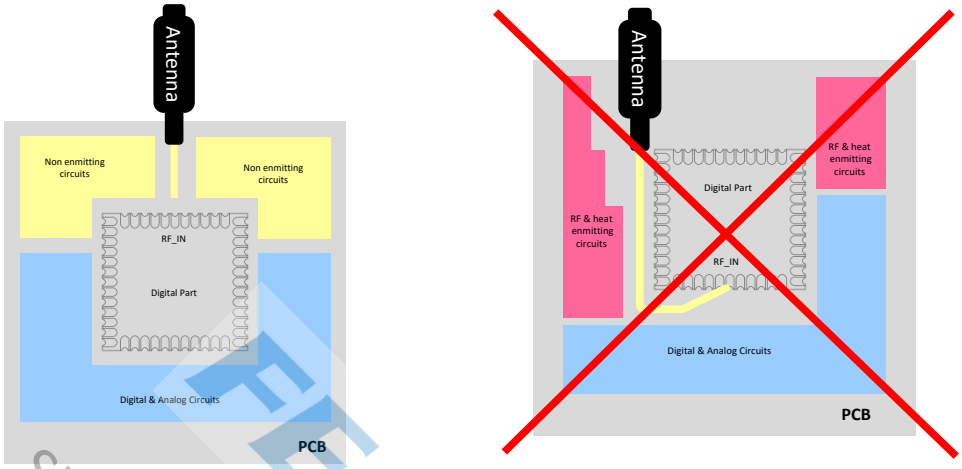


Figure 9: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

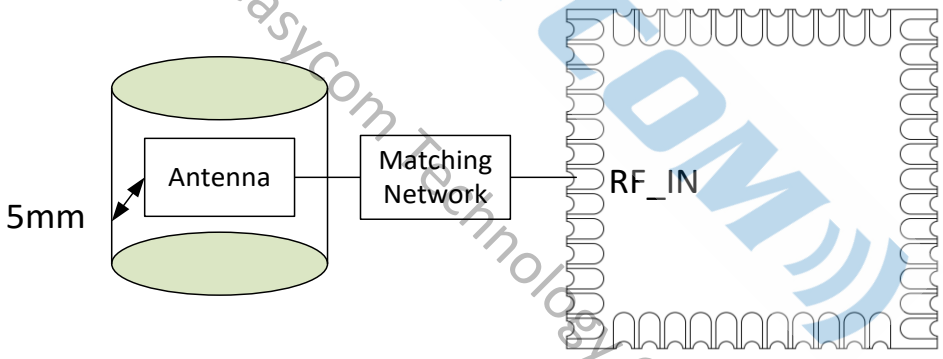


Figure 10: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

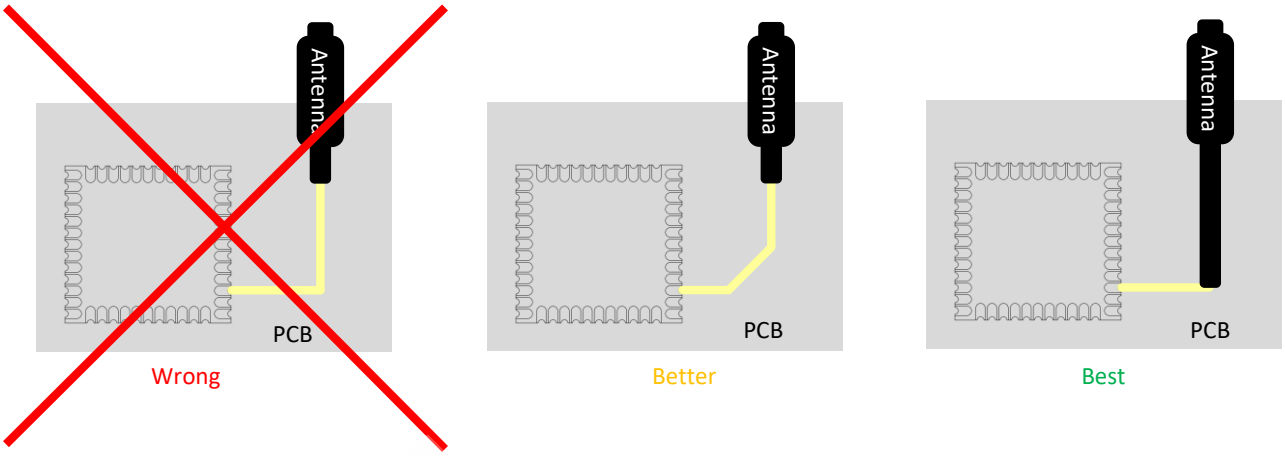


Figure 11: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

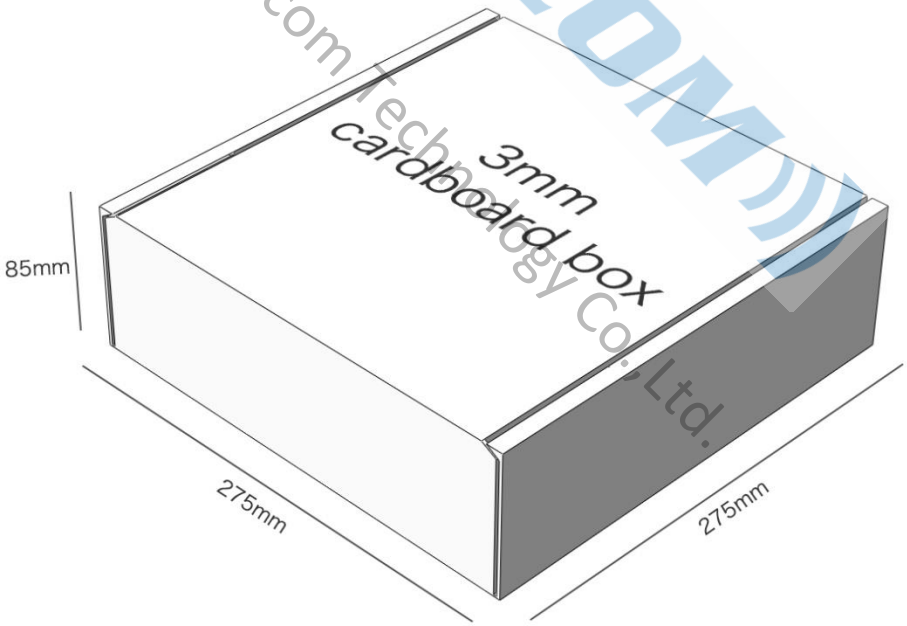
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 12: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 13: Packing Box

11. CERTIFICATION

11.1 Certificate picture

Has passed SRRC、FCC、CE and BQB certification.

SRRC：

无线电发射设备
Radio Transmission Equipment
型号核准证
Type Approval Certificate

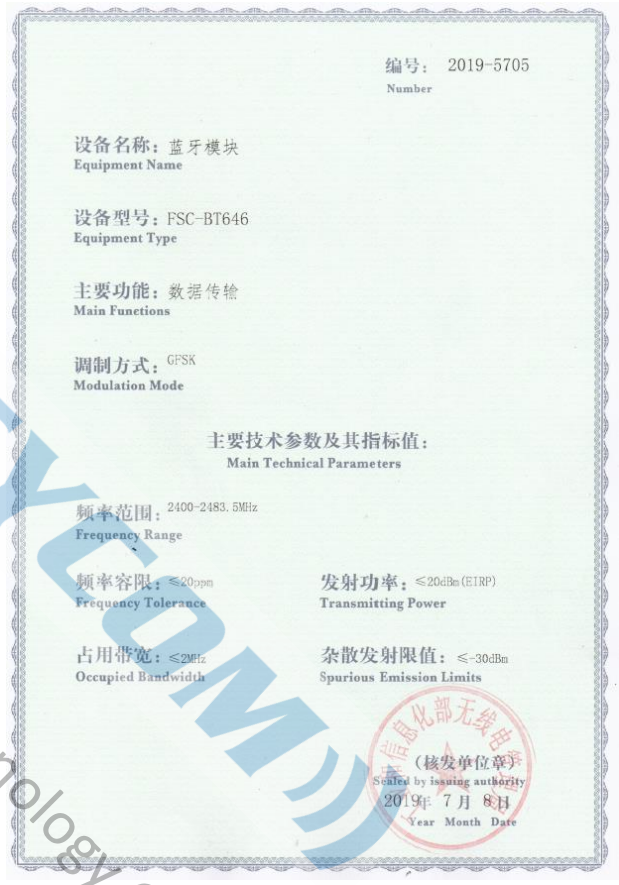
深圳市飞易通科技有限公司：

根据《中华人民共和国无线电管理
In accordance with the provisions on the Radio
条例》，经审查，下列无线电发射设备
Regulations of the People's Republic of China , the following
符合中华人民共和国无线电管理规定和
radio transmission equipment , after examination , conforms
技术标准，其核准代码为：CMIIT ID:2019DP5705
to the provisions with its CMIIT ID:

中华人民共和国工业和信息化部
（发证机关）
Sealed by issuing authority

有效期：五年
Validity

2019年 7月 8日
Year Month Date



编号： 2019-5705
Number

设备名称：蓝牙模块
Equipment Name

设备型号：FSC-BT646
Equipment Type

主要功能：数据传输
Main Functions

调制方式：GFSK
Modulation Mode

主要技术参数及其指标值：
Main Technical Parameters

频率范围：2400-2483.5MHz
Frequency Range

频率容限：≤20ppm
Frequency Tolerance

发射功率：≤20dBm(EIRP)
Transmitting Power

占用带宽：≤2MHz
Occupied Bandwidth

杂散发射限值：≤-30dBm
Spurious Emission Limits

中华人民共和国工业和信息化部无线电
（核发单位章）
Sealed by issuing authority

2019年 7月 8日
Year Month Date

BQB:

Bluetooth

Project Details

Project Name	Bluetooth Module (FSC-BT646)
Product Type	End Product
TCRL Version:	TCRL 2018-2
Referenced Qualified Design(s)	
Previously Qualified Design Used in this Qualification(s)	127815
Listing Date	2019-09-24
Declaration ID	D047850

Product Listing(s)

Name	Website	Category	Publish Date	Model Number	Description
Feasycom Bluetooth Module		Unique Products	9/24/2019 12:00:00 AM	FSC-BT646	Bluetooth Module

Member Company	Shenzhen Feiyitong Electronic Technology Co., Ltd.
Declaring Member Contact / Listing Contact Person	Name
	Address
	City
	State
	Country
	Postal Code

FCC:

TCB

GRANT OF EQUIPMENT AUTHORIZATION

Certification

Issued Under the Authority of the Federal Communications Commission By:

Eurofins Product Service GmbH
Storkower Strasse 38c
D-15526 Reichenwalde,
Germany

TCB

Date of Grant: 09/01/2019

Application Dated: 09/01/2019

Shenzhen Feasycom Technology Co.,Ltd
Room 2004A, 20th Floor, Huichao Technology
Building, Jinhai Road, Xixiang, Baoan District,,
Shenzhen,
China

Attention: Wan Zhifu

NOT TRANSFERABLE

EQUIPMENT AUTHORIZATION is hereby issued to the named GRANTEE, and is VALID ONLY for the equipment identified hereon for use under the Commission's Rules and Regulations listed below.

FCC IDENTIFIER:	2AMWOFSC-BT646
Name of Grantee:	Shenzhen Feasycom Technology Co.,Ltd
Equipment Class:	**Digital Transmission System**
Notes:	**Bluetooth module**
Modular Type:	**Single Modular**

Grant Notes	FCC Rule Parts	Frequency Range (MHZ)	Output Watts	Frequency Tolerance	Emission Designator
	15C	**2402.0 - 2480.0**	**0.0041**		

Power listed is conducted. Singular Modular Approval. Compliance of this device in all final host configurations is the responsibility of the Grantee. OEM integrators and end-users must be provided with specific operating instructions for satisfying RF exposure compliance. OEM integrators are instructed to ensure that the end user has no manual instructions to remove or install the device. SAR evaluation is valid for portable applications with an minimum distance of 5mm to human bodies.

CE:

Attestation of Global Compliance
Recognized by China National Accreditation Service for Conformity Assessment & Taiwan Accreditation Foundation

T: 0086-755-2908 1955
F: 0086-755-2600 8484
E-mail: agc@agc-cert.com
Web: Http://www.agc-cert.com

1-2/F, Building 19, Junfeng Industrial Park
Chongqing Road, Heping Community, Fuhai Street
Bao 'an District, Shenzhen, Guangdong, China

EU-RED Certificate of Conformity

Radio Equipment Directive (RED) 2014/53/EU

Registration No.	AGC03285190801E0
Applicant	Shenzhen Feasycom Technology Co., LTD Room 2004A, 20th Floor, Huichao Technology Building, Jinhai Road, Xixiang , Baoan District, Shenzhen, China
Product Designation	Bluetooth module
Brand Name	Feasycom
Model / Series Models	FSC-BT646
Manufacturer	Shenzhen Feasycom Technology Co., LTD Room 2004A, 20th Floor, Huichao Technology Building, Jinhai Road, Xixiang , Baoan District, Shenzhen, China

Requirement	Applied Standards	Document Evidence	Result
Art.3.1(a) Health	EN 62479:2010	Test Report: AGC03285190801EH02	Conform
Art.3.1(a) Safety	EN 60950-1:2006+A11:2009 +A1:2010+A12:2011+A2:2013	Test Report: AGC03285190801ES01	Conform
Art.3.1(b) EMC	Draft EN 301 489-1 V2.2.1 Draft EN 301 489-17 V3.2.0	Test Report: AGC03285190801EE02	Conform
Art.3.2 Radio	EN 300 328 V2.1.1	Test Report: AGC03285190801EE11	Conform

CE

Signed by General Manager(King Zhang)
Issue Date: Aug. 29, 2019

Recognized by Attestation of Global Compliance (Shenzhen) Co., Ltd., in accordance with the RED Directive 2014/53/EU. The certificate doesn't imply assessment of the production. The Applicant of the certificate is authorized to use this certificate in connection with EC declaration of conformity to the Directive. The certificate is only applicable to the equipments described above. This certificate shall not be re-produced except in full without the written approval of Attestation of Global Compliance (Shenzhen) Co., Ltd.
Note: This certificate is part of the full test report(s) and should be used in conjunction with it.

Version: 2.0

12. APPLICATION SCHEMATIC