Specification for EPD

Model NO. : W021A01

Prepared by	Checked by	Approved by

Customer approval

Customer	Approved by	Date of Approval

Version	Content	Date	Producer
A/0	New Release	2019/07/07	WJ
A/1	Change the IC	2020/05/16	WSZ

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1 General Description

W021A01 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference systemdesign. The 2.13” active area contains 104x212 pixels, and has 2-bit full display capabilities. The module is aTFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCUinterface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable
electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- 104×212pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^{2}C signal master interface to read extemal temperature sensor

3 Application

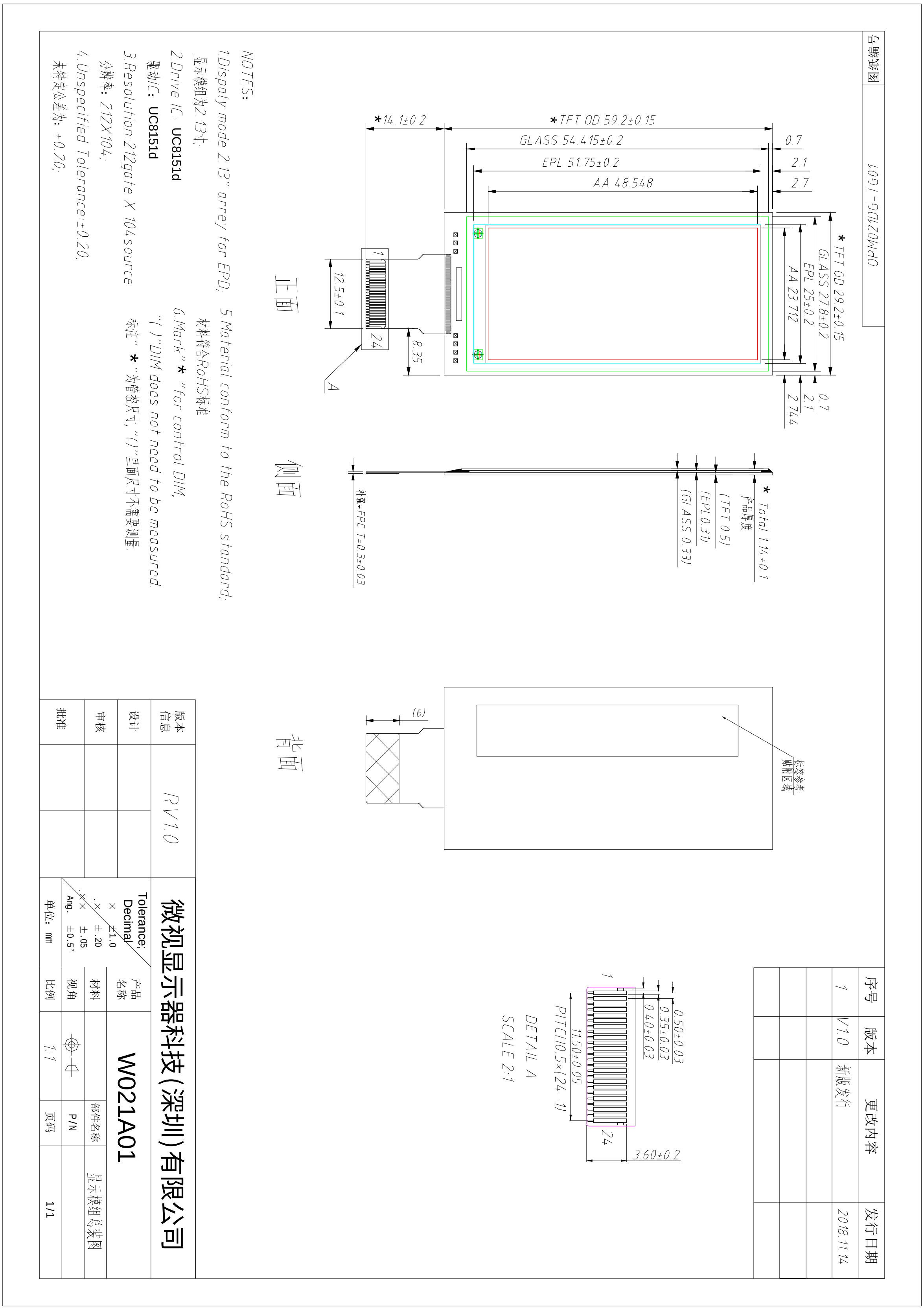
Electronic Shelf Label System

4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit
Screen Size	2.13	Inch
Display Resolution	104(H)×212(V)	Pixel
Active Area	23.712×48.548	mm
Pixel Pitch	0.228×0.229	mm
Pixel Configuration	Rectangle	
Outline Dimension	29.2(H)×59.2 (V) ×1.14(D)	mm
Weight	4.1	g

4.2 Mechanical Drawing of EPD Module


NOTES:
1.Dispaly mode 2.13" arrey for EPD,
显示模组为2.13寸;
2.Drive IC: UC8151d
驱动IC: UC8151d
3.Resolution:212gate X 104source
分辨率: 212X104;
4.Unspecified Tolerance:±0.20;
未特定公差为: ±0.20;
5.Material conform to the RoHS standard;
材料符合RoHS标准
6.Mark "*" for control DIM,
"( )"DIM does not need to be measured
标注"*"为管控尺寸,"( )"里面尺寸不需要测量
正面
侧面
背面
*14.1±0.2
*TFT OD 59.2±0.15
GLASS 54.415±0.2
EPL 51.75±0.2
AA 48.548
0.7
2.1
2.7
*TFT OD 29.2±0.15
GLASS 27.8±0.2
EPL 25±0.2
AA 23.712
2.744
12.5±0.1
8.35
1
24
A
补强+FPC T=0.3±0.03
*Total 1.14±0.1
产品厚度
(TFT 0.5)
(EPL 0.31)
(GLASS 0.33)
(6)
0.50±0.03
0.35±0.03
0.40±0.03
11.50±0.05
PITCH0.5×(24-1)
3.60±0.2
DETAIL A
SCALE 2:1
版本信息
RV1.0
设计
审核
批准
微视显示器科技(深圳)有限公司
产品名称
W021A01
材料
视角
比例
1:1
部件名称
显示模组总装图
P/N
页码
1/1
Tolerance:
Decimal
× ±1.0
.× ±.20
.×× ±.05
Ang. ±0.5°
单位: mm
序号
版本
更改内容
发行日期
1
V1.0
新版发行
2018.11.14

5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS State	**MCU Interface**
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	**Symbol**	**Rating**	**Unit**
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{dd} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{dd} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25°C.

Parameter	**Symbol**	**Condition**	**Applicable pin**	**Min.**	**Typ.**	**Max.**	**Unit**
Logic supply voltage	V_{dd}	-	VDD	2.2	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{dd}	V
OTP Program voltage	V_{PP}	-	VPP	-	7.5	-	V
Typical power panel	P_{TYP}	-	-	-	12	30	mW
Deep sleep mode	P_{STPY}	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	V_{dd} =3.0V-	-	-	4.0	10	mA

Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	20	--	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	--	uA
Operation temperature range	T_{OPR}	-	-	0	-	50	°C
Operation relative humidity	RHop	-	-	-	-	70	%RH
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature range	T_{STG}	-	-	0	-	50	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition:from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

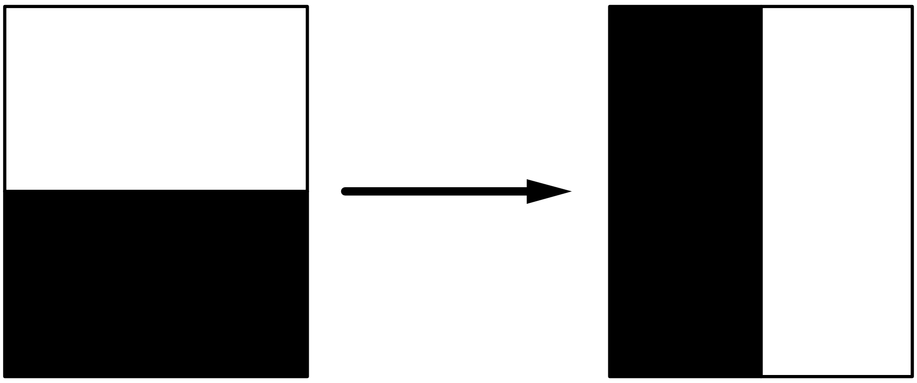


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25℃.

Parameter	**Symbol**	**Condition**	**Applicable pin**	**Min.**	**Typ.**	**Max.**	**Unit**
VCOM output voltage	VCOM	-	VCOM	-3.0	-	-0.2	V
Positive Source output voltage	V_{SH}	-	S0-103	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	S0-103	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	g0-g211	+21	+22	+23	V
Negative gate output voltage	Vgl	-	g0-g211	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	**Data/Connnand Interface**		**Control Signal**		
Bus interface	**SDA**	**SCL**	**CSB**	**D/C**	**RSTN**
4-wire SPI	SDIN	SCLK	**CSB**	D/C	RSTN
3-wire SPI	SDIN	SCLK	**CSB**	L	RSTN

Table 10-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	**CSB**	**D/C**	**SCLK**
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

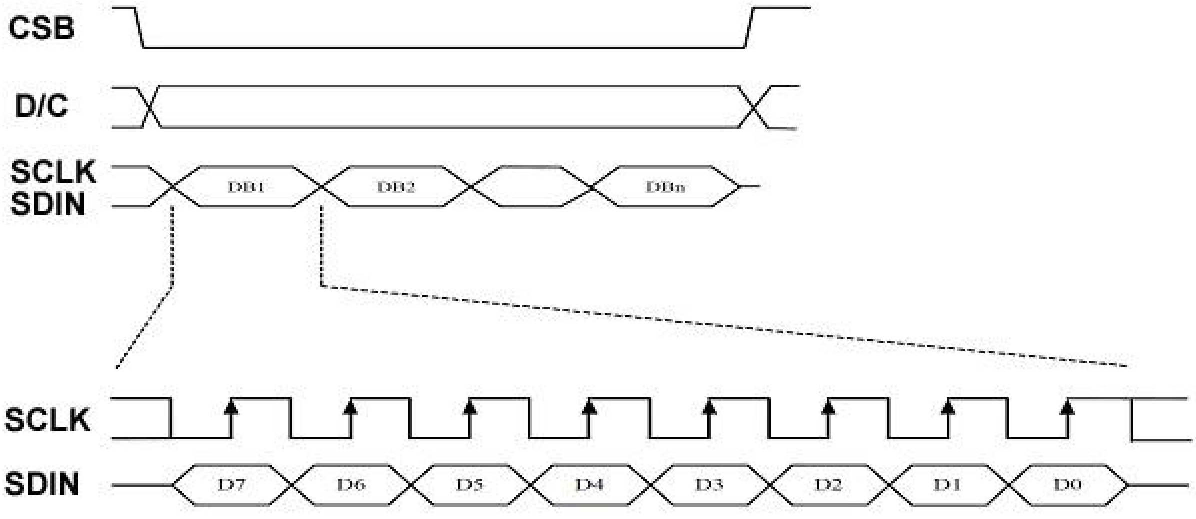


Figure 10-4-2: Write procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

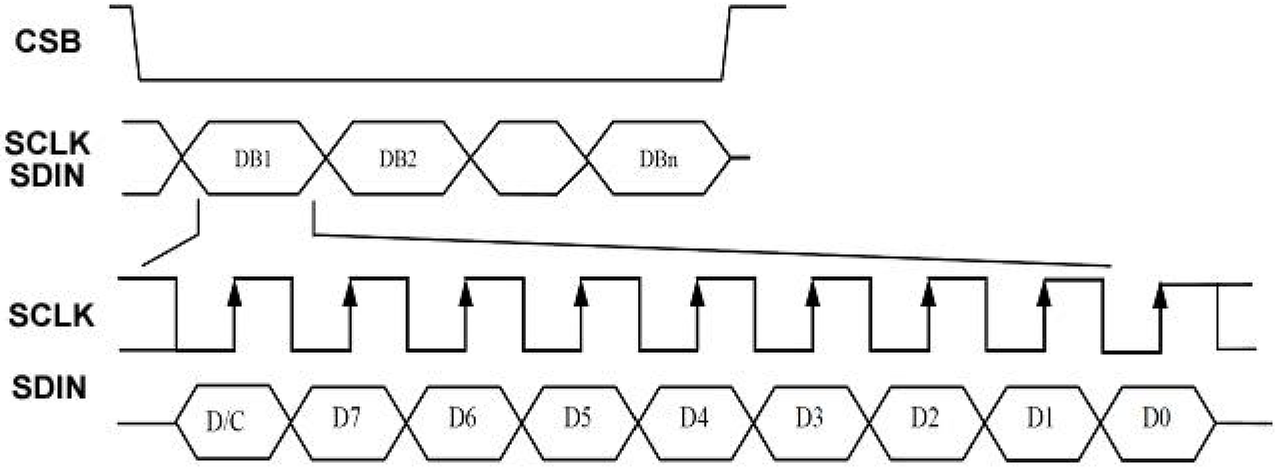


Figure 10-4-3: Write procedure in 3-wire SPI mode

6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25ºC.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	**VDD** =2.4 to 3.3V	CL	0.95	1	1.05	MHz

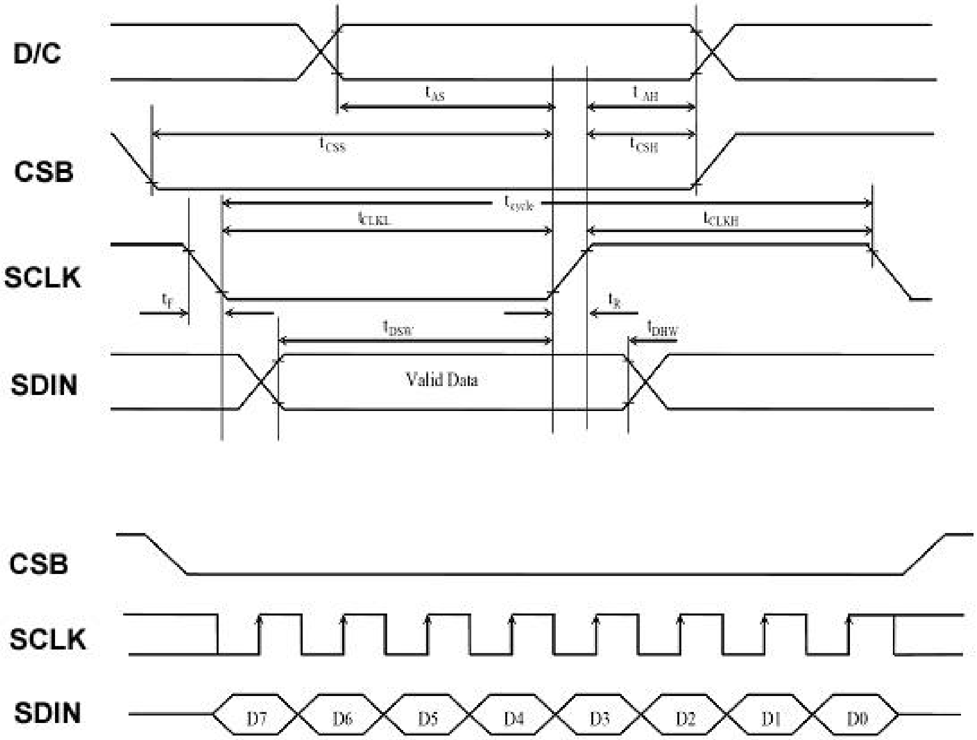

D/C
CSB
SCLK
SDIN
tAS
tAH
tCSS
tCSH
tcycle
tCLKL
tCLKH
tF
tR
tDSW
tDHW
Valid Data
CSB
SCLK
SDIN
D7
D6
D5
D4
D3
D2
D1
D0

Figure 10-4-4: Serial interface characteristics

(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

Table 10-4-4: Serial Interface Timing Characteristics

6.4.5 Command Table

R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[8:0] = 127h Set B[2:0] = 0h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Set A[7:0] = 8Bh Set B[7:0] = 9Ch Set C[7:0] = 96h Set D[7:0] = 0Fh
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A_0		A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.

R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh[POR]
0	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
0	1		A_3	A_2	A_1	A_0	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1		A_7	0	0	A_4	A_3	A_2	A_1	A_0		

<table>
<tr><th>R/W#</th><th>D/C</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
<table>
<tr><th></th><th>Parameter (in Hex)</th></tr>
<tr><td>Enable Clock Signal,
Then Enable Analog
Then Load Temperature Sensor
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF
[POR]</td></tr>
<tr><td>**Setting for LUT from OTP according to external Temperature Sensor operation 2**
Enable Clock Signal,
Then Enable Analog
Then Load LUT
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>D7</td></tr>
<tr><td>**Setting for LUT from MCU**
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly

For Write pixel:
Content of Write RAM= 1
For Black pixel:
Content of Write RAM = 0</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Write VCOM register</td><td rowspan="2">Write VCOM register from MCU interface
A[7:0] = 00h [POR]
<table>
<tr><th>A[7:0]</th><th>vcom</th><th>A[7:0]</th><th>vcom</th></tr>
<tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr>
<tr><td>0Bh</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr>
<tr><td>10h</td><td>-0.4</td><td>4Bh</td><td>-1.9</td></tr>
<tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr>
<tr><td>17h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr>
<tr><td>1Bh</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr>
<tr><td>20h</td><td>-0.8</td><td>5Bh</td><td>-2.3</td></tr>
<tr><td>24h</td><td>-0.9</td><td>5Fh</td><td>-2.4</td></tr>
<tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr>
<tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr>
<tr><td>2Fh</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr>
<tr><td>34h</td><td>-1.3</td><td>6Fh</td><td>-2.8</td></tr>
<tr><td>37h</td><td>-1.4</td><td>73h</td><td>-2.13</td></tr>
<tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr>
<tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Write LUT register</td><td rowspan="2">Write LUT register from MCU interface
[70 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]).
Refer to Session 6.7Waveform Setting</td></tr>
<tr><td>0
0
0
…
0
0</td><td>1
1
1
…
1
1</td><td></td><td colspan="8">LUT
[70 bytes]</td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Set dummy line period</td><td rowspan="2">Set A[6:0] = 00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Set Gate line width</td><td>Set A[3:0] = 09h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td>Select border waveform for VBD</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td>A[7:0] = C0h [POR], set VBD as HIZ.

A [7:6] :Select VBD option
<table>
<tr><td>A[7:6]</td><td>Select VBD as</td></tr>
<tr><td>00</td><td>GS Transition
Defined in A[1:0]</td></tr>
<tr><td>01</td><td>Fix Level
Defined in A[5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11[POR]</td><td>HiZ</td></tr>
</table>
A [5:4] Fix Level Setting for VBD
<table>
<tr><td>A[5:4]</td><td>VBD level</td></tr>
<tr><td>00[POR]</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11</td><td>VSH2</td></tr>
</table>
A [1:0] GS Transition setting for VBD
<table>
<tr><td>A[1:0]</td><td>VBD Transition</td></tr>
<tr><td>00[POR]</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table>
</td></tr>
</table>

R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 13h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
White△L 24h	Reduce		-	≤4	-	-	-
T_{update}	Image update time	at 25 °C	-	2100	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8 Handling, Safety, and Environment Requirements

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

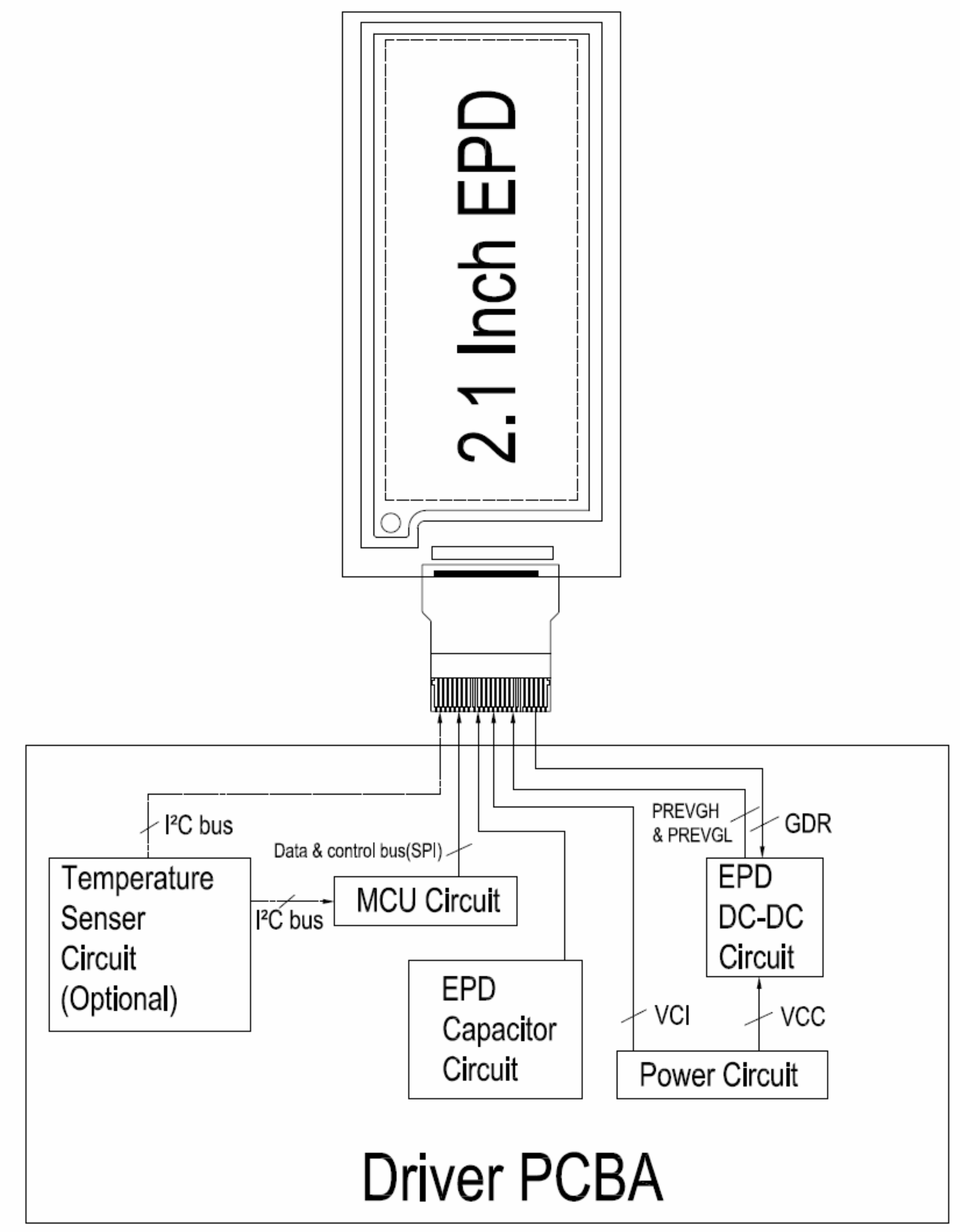
Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

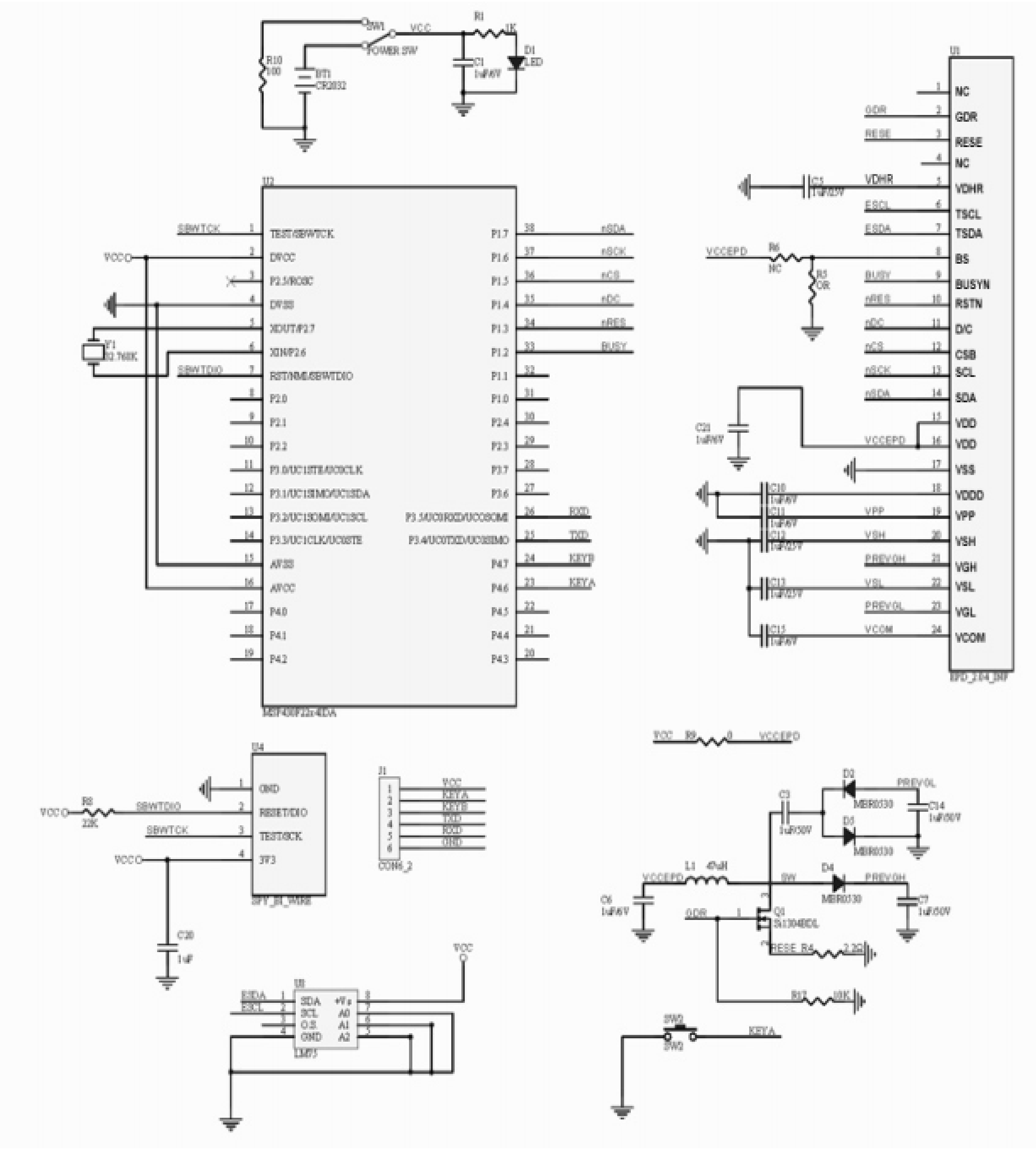
9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

10 Block Diagram


2.1 Inch EPD
I²C bus
Data & control bus(SPI)
PREVGH
& PREVGL
GDR
Temperature
Senser
Circuit
(Optional)
I²C bus
MCU Circuit
EPD
DC-DC
Circuit
EPD
Capacitor
Circuit
VCI
VCC
Power Circuit
Driver PCBA

11 Typical Application Circuit with SPI Interface


SW1
VCC
R1
1K
POWER SW
R10
100
BT1
CR2032
C1
1uF/6V
D1
LED
U2
SBWTCK
TEST/SBWTCK
VCC
DVCC
P2.5/ROSC
DVSS
XOUT/P2.7
XIN/P2.6
Y1
32.768K
SBWTDIO
RST/NMI/SBWTDIO
P2.0
P2.1
P2.2
P3.0/UC1STE/UC0CLK
P3.1/UC1SIMO/UC1SDA
P3.2/UC1SOMI/UC1SCL
P3.3/UC1CLK/UC0STE
AVSS
AVCC
P4.0
P4.1
P4.2
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P2.4
P2.3
P3.7
P3.6
P3.5/UC0RXD/UC0SOMI
P3.4/UC0TXD/UC0SIMO
P4.7
P4.6
P4.5
P4.4
P4.3
nSDA
nSCK
nCS
nDC
nRES
BUSY
RXD
TXD
KEYB
KEYA
MSP430F22x4DA
U1
NC
GDR
RESE
NC
VDHR
TSCL
TSDA
BS
BUSYN
RSTN
D/C
CSB
SCL
SDA
VDD
VDD
VSS
VDDD
VPP
VSH
VGH
VSL
VGL
VCOM
EPD_2.04_INF
C5
1uF/25V
ESCL
ESDA
VCCEPD
R6
NC
R5
0R
C21
1uF/6V
C10
1uF/6V
C11
1uF/6V
C12
1uF/25V
C13
1uF/25V
C15
1uF/6V
VPP
VSH
PREVGH
VSL
PREVGL
VCOM
VCC
R9
0
VCCEPD
U4
GND
RESET/DIO
TEST/SCK
3V3
R8
22K
SBWTDIO
SBWTCK
C20
1uF
SPY_BI_WIRE
J1
VCC
KEYA
KEYB
TXD
RXD
GND
CON6_2
D2
PREVGL
C3
1uF/50V
MBR0330
C14
1uF/50V
D3
MBR0330
L1
47uH
VCCEPD
SW
D4
MBR0330
PREVGH
C6
1uF/6V
C7
1uF/50V
GDR
Q1
Si1304BDL
RESE
R4
2.2Ω
R12
10K
U3
ESDA
ESCL
SDA
SCL
O.S.
GND
+Vs
A0
A1
A2
LM75
SW2
KEYA

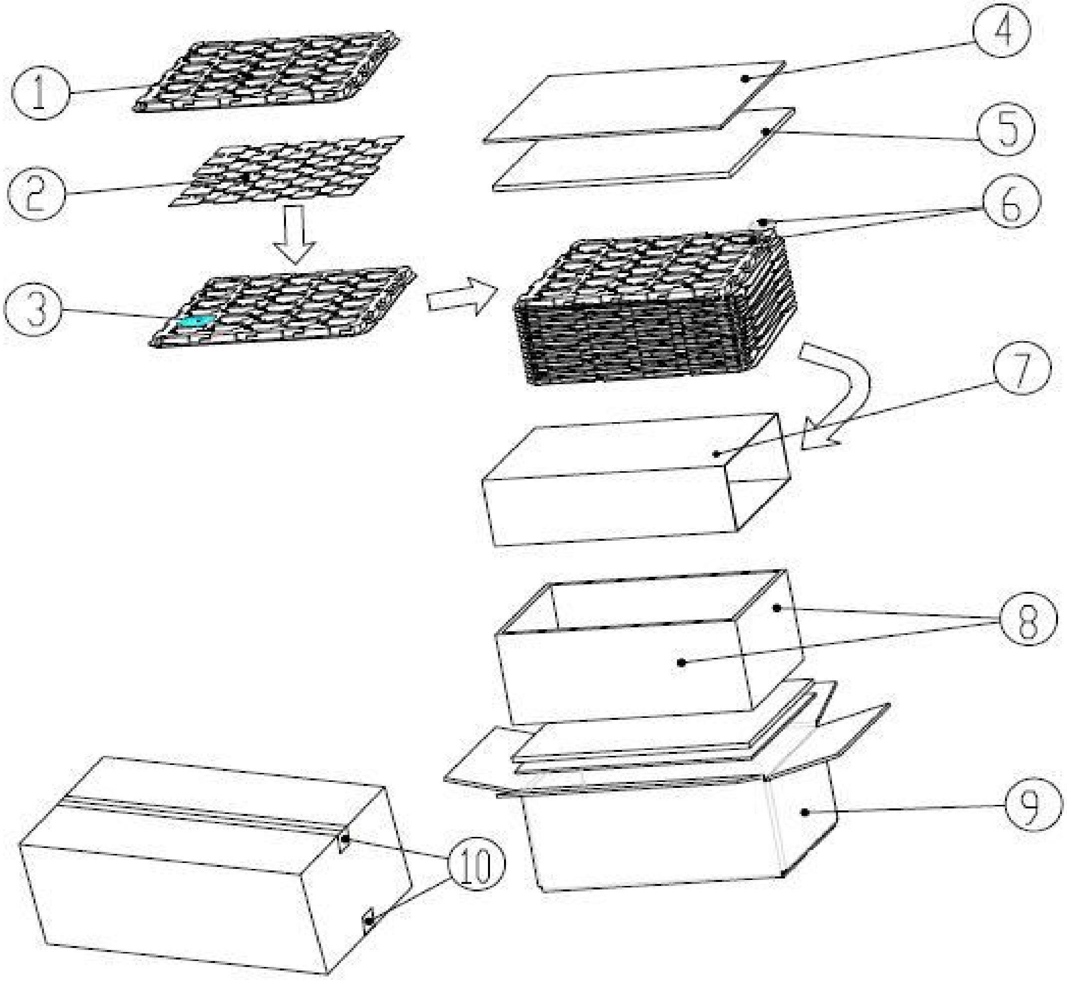
12 Packaging

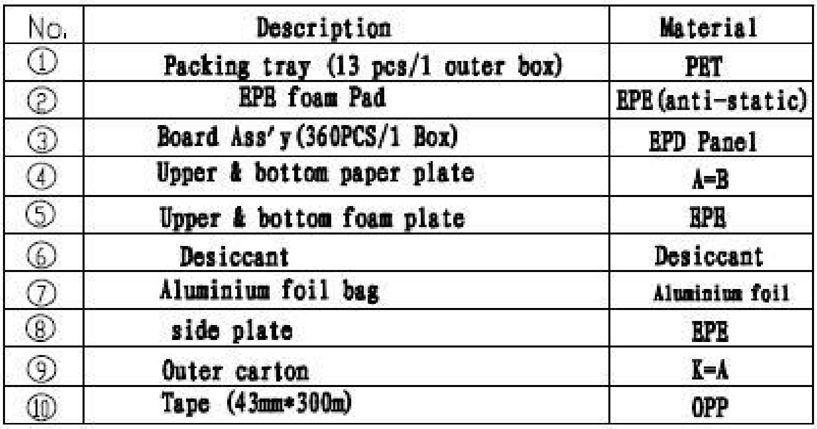
Packing Form

a) Package quantity in one outer box:360 pcs

b) box size:470 mm X 322 mm X 170 mm

c) 1 outer box = 12 (full tray) + 1 (dummy / top tray)





No.	Description	Material
①	Packing tray (13 pcs/1 outer box)	PET
②	EPE foam Pad	EPE(anti-static)
③	Board Ass'y(360PCS/1 Box)	EPD Panel
④	Upper & bottom paper plate	A=B
⑤	Upper & bottom foam plate	EPE
⑥	Desiccant	Desiccant
⑦	Aluminium foil bag	Aluminium foil
⑧	side plate	EPE
⑨	Outer carton	K=A
⑩	Tape (43mm*300m)	OPP

13 Mark and Bar Code Definition

W021A01 MMMMMMMM XX

R5F086AN1001001

(A) W021A01 : Module No.

(B) MMMMMMMM: Product date year month day

(C) XX: Internal Code

(D) Bar Code definition

R5F086	A	N1	001	001
（1）	（2）	（3）	（4）	（5）

(1) O-Paper Film LOT

(2) Factory

(3) Internal Code

(4) Product LOT

(5) Product Serial Number